

# PALAU

CPU : Intel Merom-4M (800/667 MHz)  
Chip Set : Intel Crestline & ICH8-M  
Remarks : Mobility Platform

Model Name : SANTA ROSA STD  
PBA Name : MAIN  
PCB Code : BA41-00753A NANYA  
PCB Code : BA41-00786A GCE  
Dev. Step : PV - 2  
Revision : 1.0  
T.R. Date : 2007. 03.30

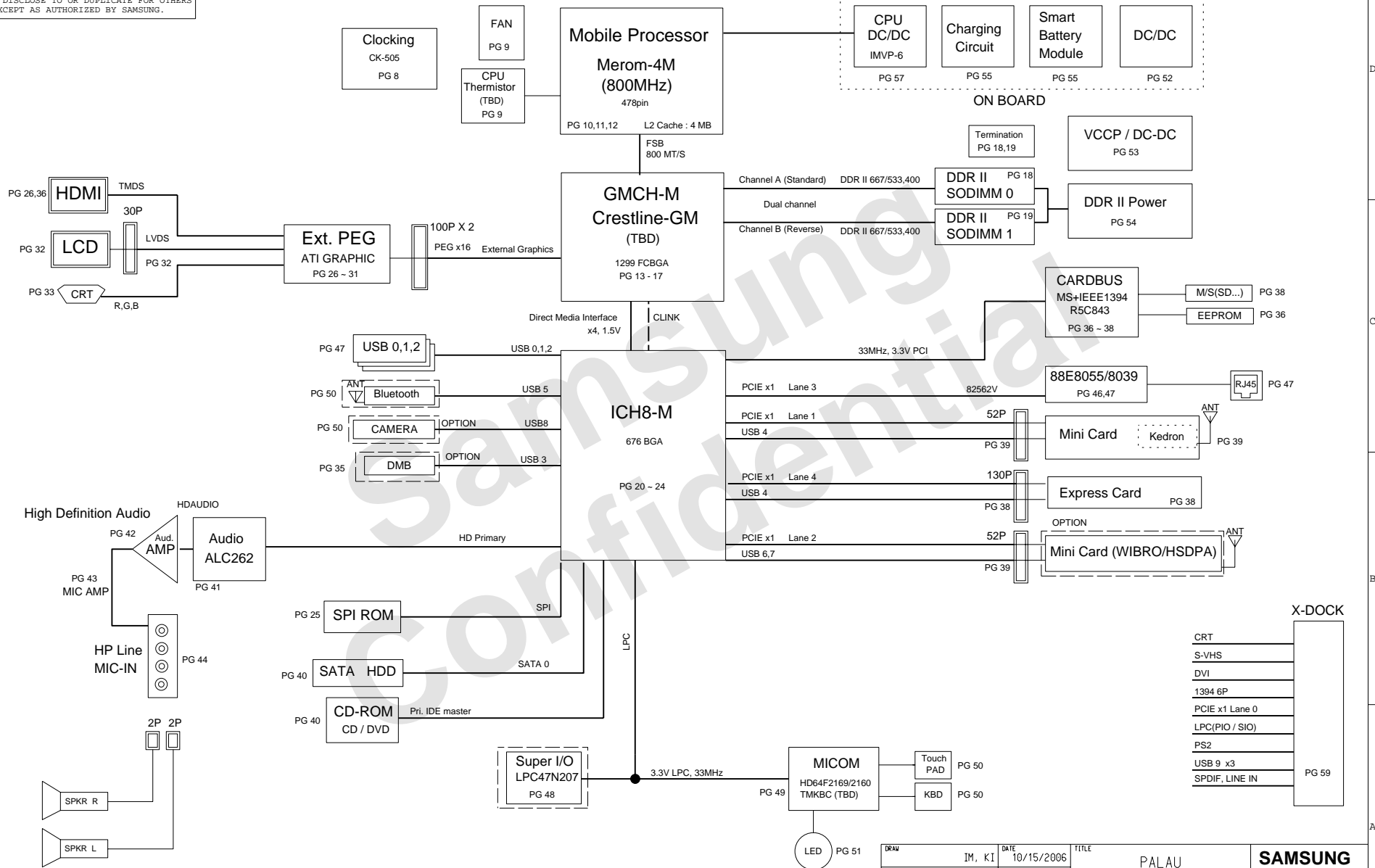
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Owner : SEC Mobile R & D Signature : X

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CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	0.7	COVER		PART NO. BA41-####A
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	1 OF 22	

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# BOARD INFORMATION

D

## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices			
Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI LPC bridge/IDE/AC97/SMBUS	AD30(internal) AD31(internal)	- -	- B
Internal MAC AC Link GLAN	AD24(internal) - -	- - -	E B F

Voltage Rails	
VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched off power rail (off in S3-S5)
P1.8V	1.8V switched off power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR
P0.9V	0.9V power rail for DDR
P3.3V	3.3V switched off power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail
P5.0V	5.0V switched off power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail
P5.0V_ALW	5.0V always power rail

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	0	DOCKING FOR GIGA LAN
1	SYSTEM PORT 1	1	Mini Card (KEDRON)
2	SYSTEM PORT 2	2	EXPRESS CARD TYPE I
3	DMB or DOCKING	3	SYSTEM FOR LAN
4	EXPRESS CARD TYPE I	4	Mini Card (WIBRO / HSDPA)
5	Bluetooth	5	RESERVED
6	WIBRO / HSDPA		
7	CAMERA		
8	USIM CONTROL FOR WIBRO		
9	MEMORY CARD CONTROLLER		

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	12.0MHz	Memory Card Controller	AUG371
Crystal	25MHz	LAN	Intel LAN

LCD Pannel Detect (TBD)		
Devices	Resolution	PANNEL_DETECT_0

I <sup>2</sup> C / SMB Address			
Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMMO	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMMO	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
MICOM	Master	-	SMBUS Master
EMC2102	0101 110X	5Ch	Thermal Sensor
BATTERY	0001 011X	16h	BATTERY

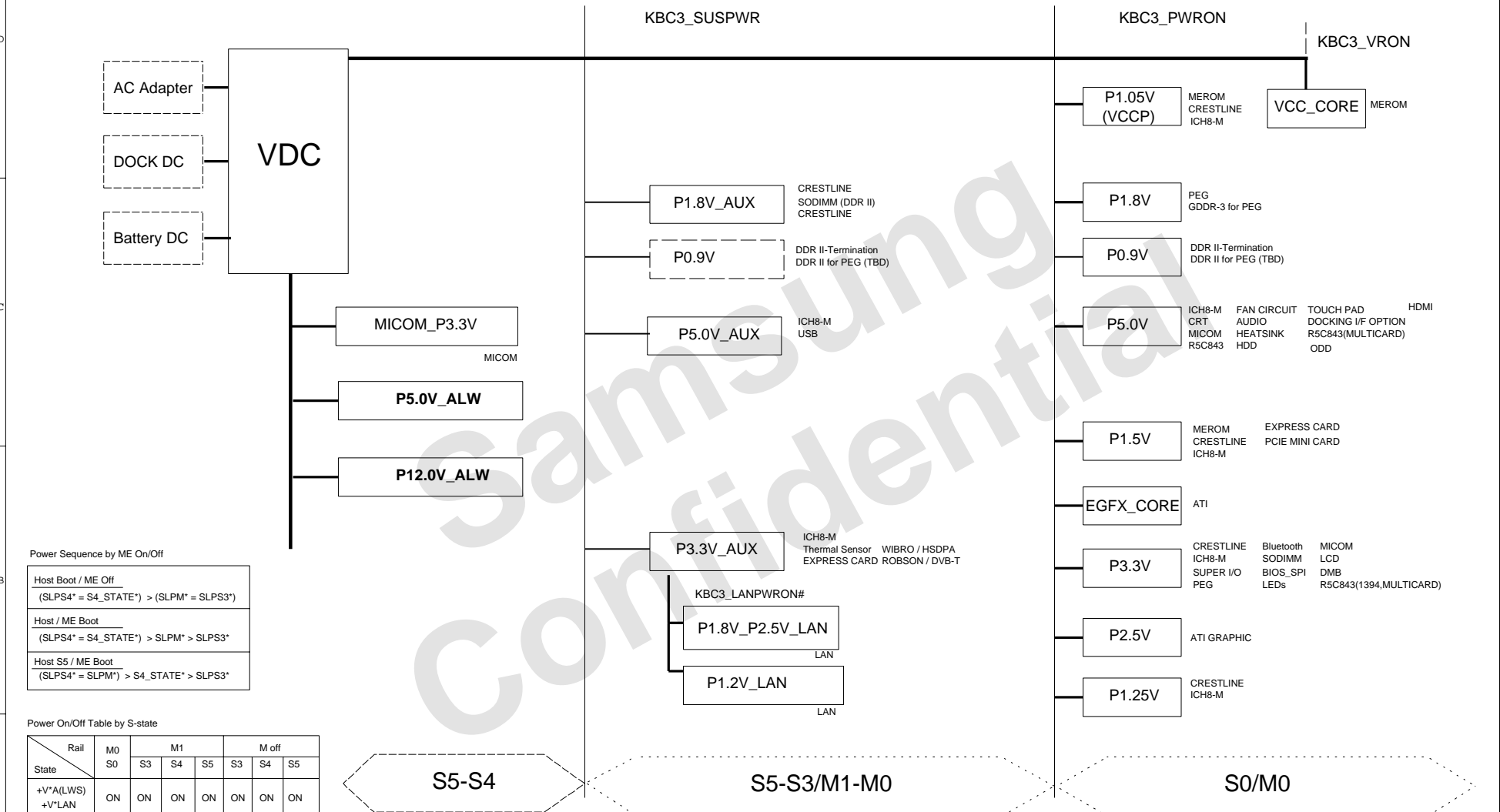
## REVISION HISTORY

See rev notes for more information.

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# POWER DIAGRAM



Power Sequence by ME On/Off

Host Boot / ME Off
(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
Host / ME Boot
(SLPS4* = S4_STATE*) > SLPM* > SLPS3*
Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

Power On/Off Table by S-state

Rail State	M0 S0	M1			M off		
		S3	S4	S5	S3	S4	S5
+V*(LWS) +V*LAN	ON	ON	ON	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	ON	ON	ON	—	—
+V*_AUX	ON	ON	—	—	ON	—	—
+V*_M	ON	ON	ON	ON	—	—	—
+V* (CORE)	ON	—	—	—	—	—	—

S5-S4

S5-S3/M1-M0

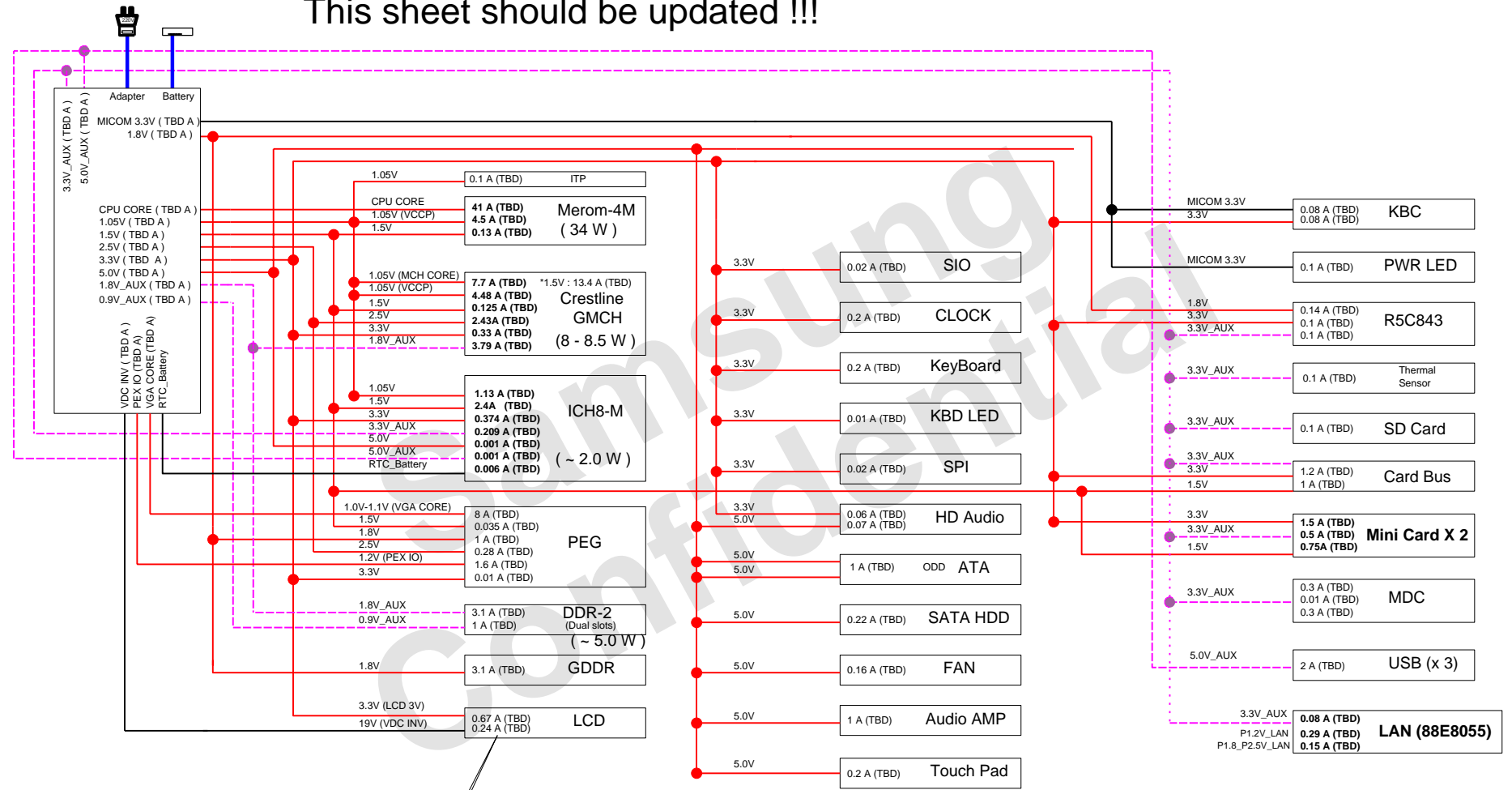
S0/M0

DRAW	IM, KI	DATE	10/15/2006	TITLE	PALAU	<b>SAMSUNG</b> ELECTRONICS
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APPROVAL	BIN, KK	REV	0.7	POWER DIAGRAM		PART NO. BA41-####A
MODULE CODE	undef ined	LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	4 OF 22	

# POWER RAILS ANALYSIS

Rev. 0.7

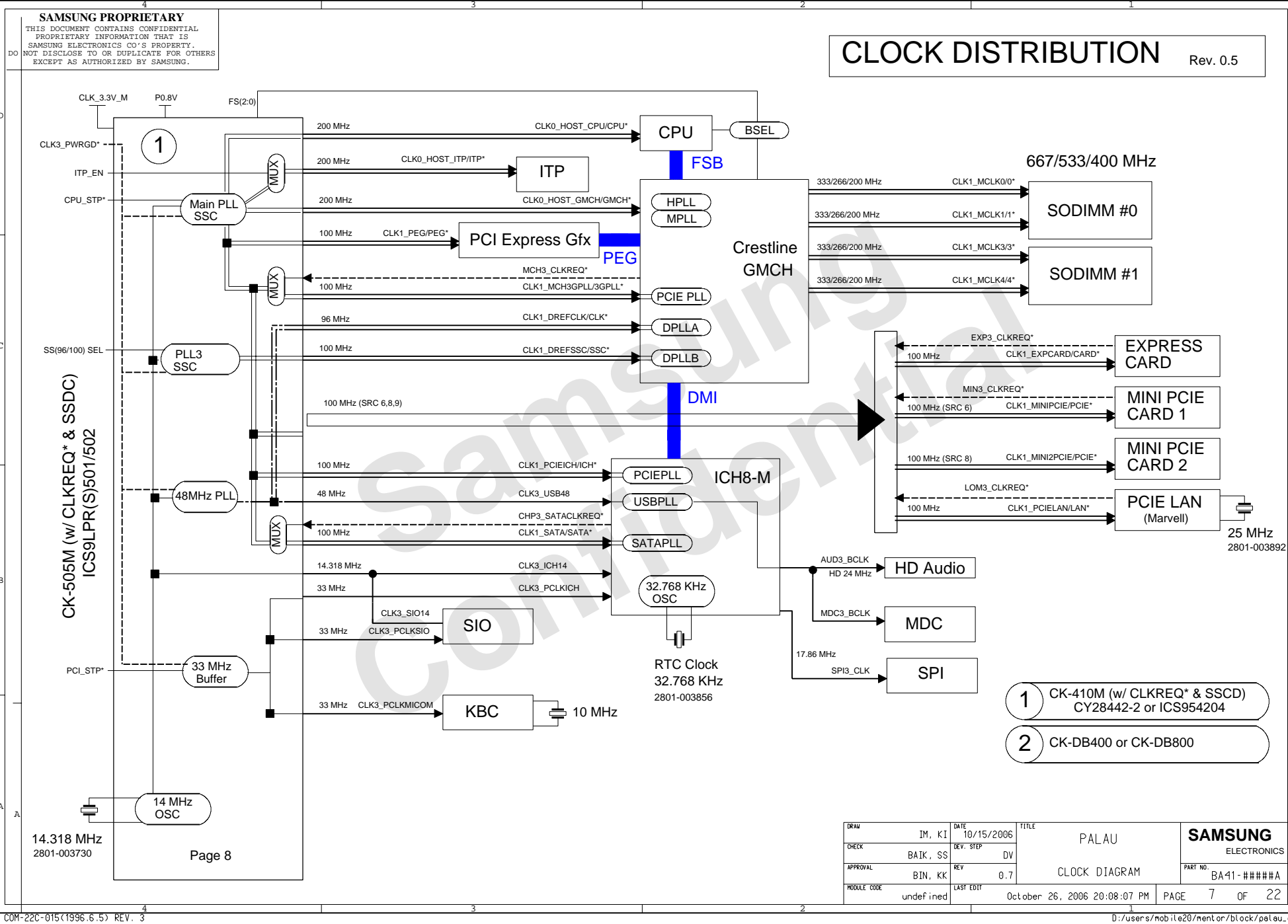
This sheet should be updated !!!



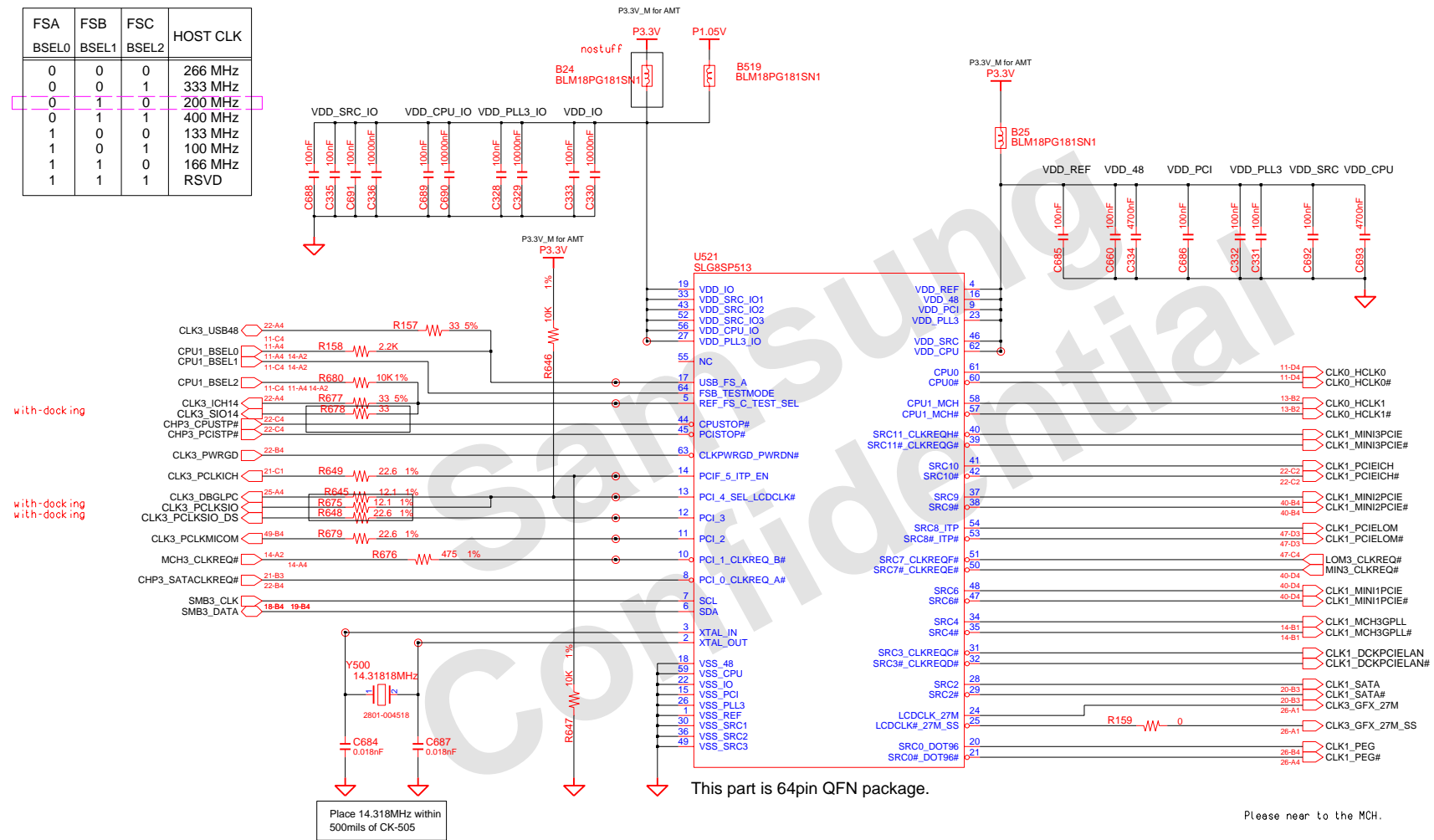
Value by Datasheet/Application notes (Value by measurement)

DRAW	IM, KI	DATE	10/15/2006	TITLE	PALAU	SAMSUNG
CHECK	BAIK, SS	DEV. STEP	DV			ELECTRONICS
APPROVAL	BIN, KK	REV	0.7		POWER RAILS	PART NO.
MODULE CODE	undef ined	LAST EDIT	October 26, 2006 20:08:07 PM			BA41-#####A
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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

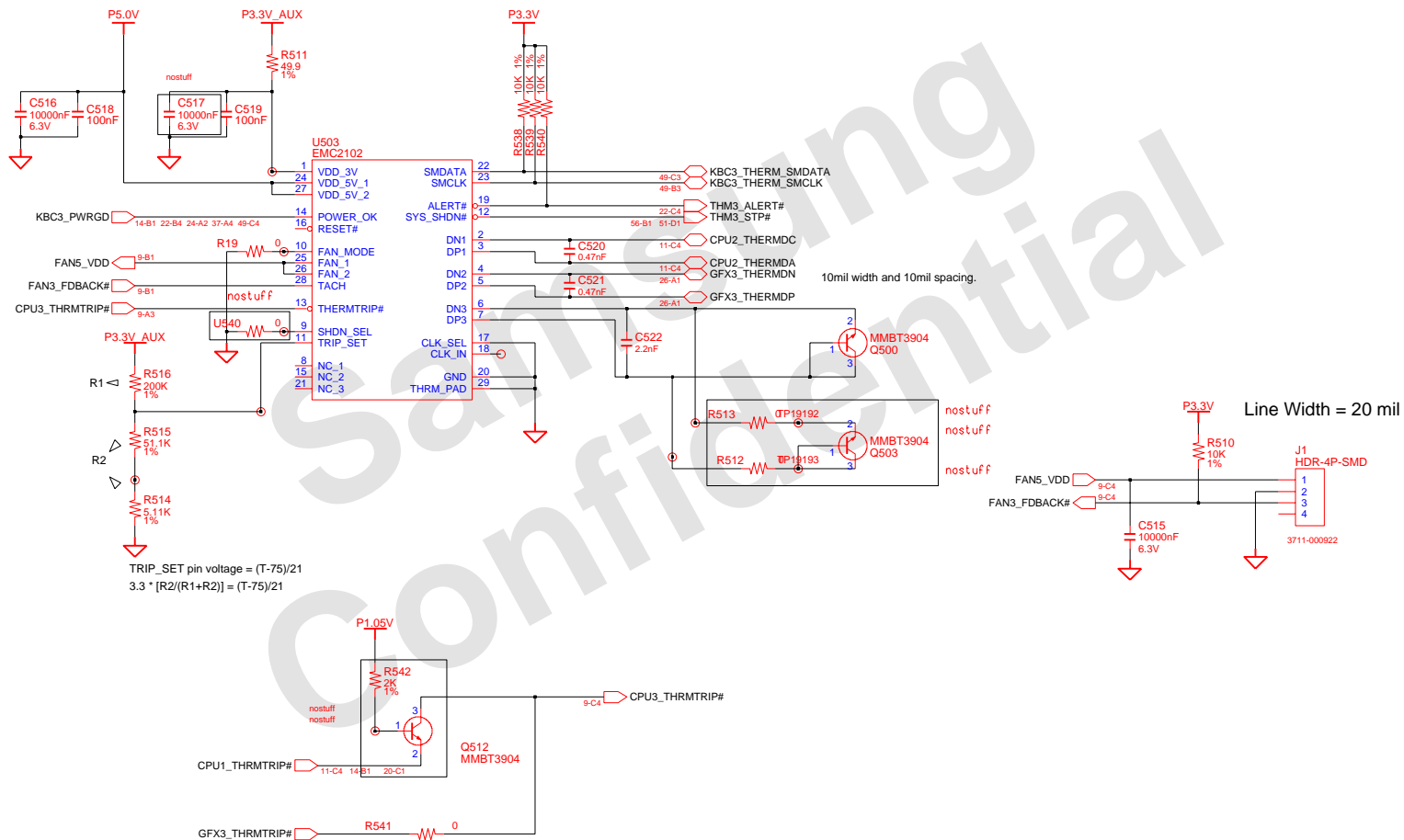


CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	LOM	SRC8

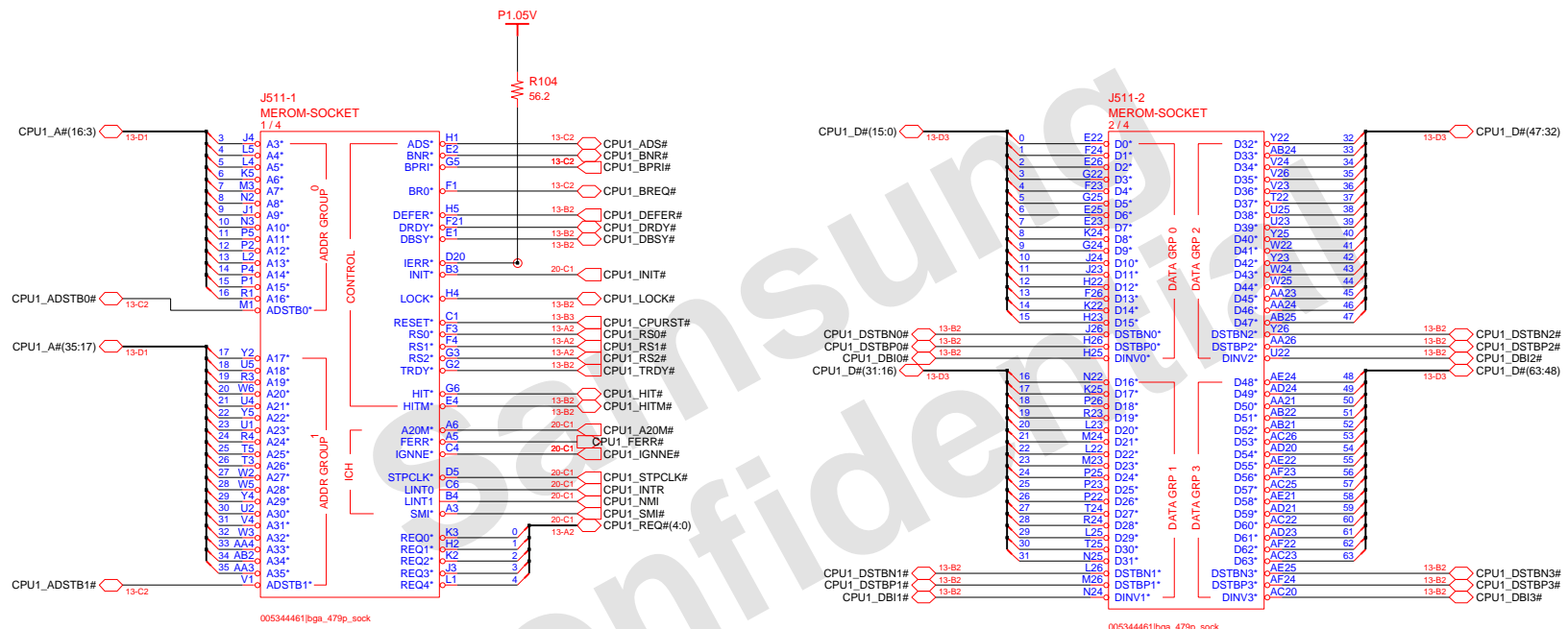
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CHECK	TF Member	DEV. STEP	DV	Main_Clock_Circuit		
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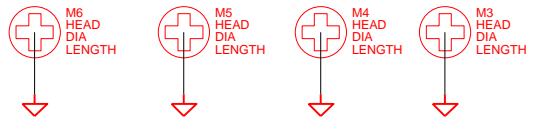
# THERMAL SENSOR & FAN CONTROL



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MODULE CODE		LAST EDIT	October 10, 2006 20:56:52 PM	PAGE	1 OF 1	

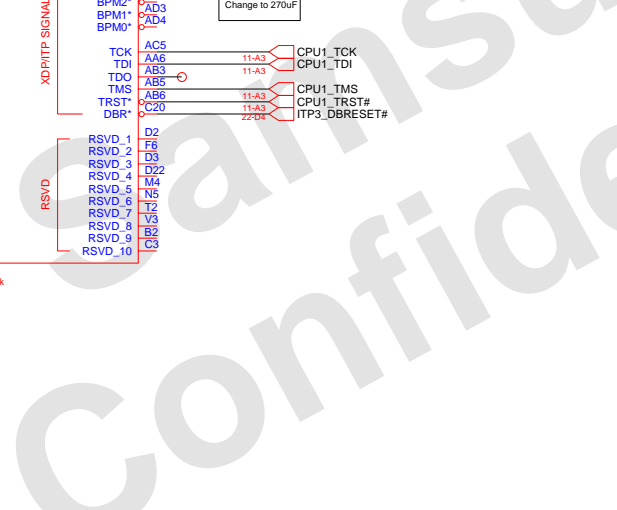


CPU HEATSINK SUPPORT HOLE



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APPROVAL	TF Member	REV	0.7		CPU_Merom_SR_SV (1/3)	
MODULE CODE	undef ined	LAST EDIT	October 13, 2006 13:49:51 PM	PAGE	1 OF 3	

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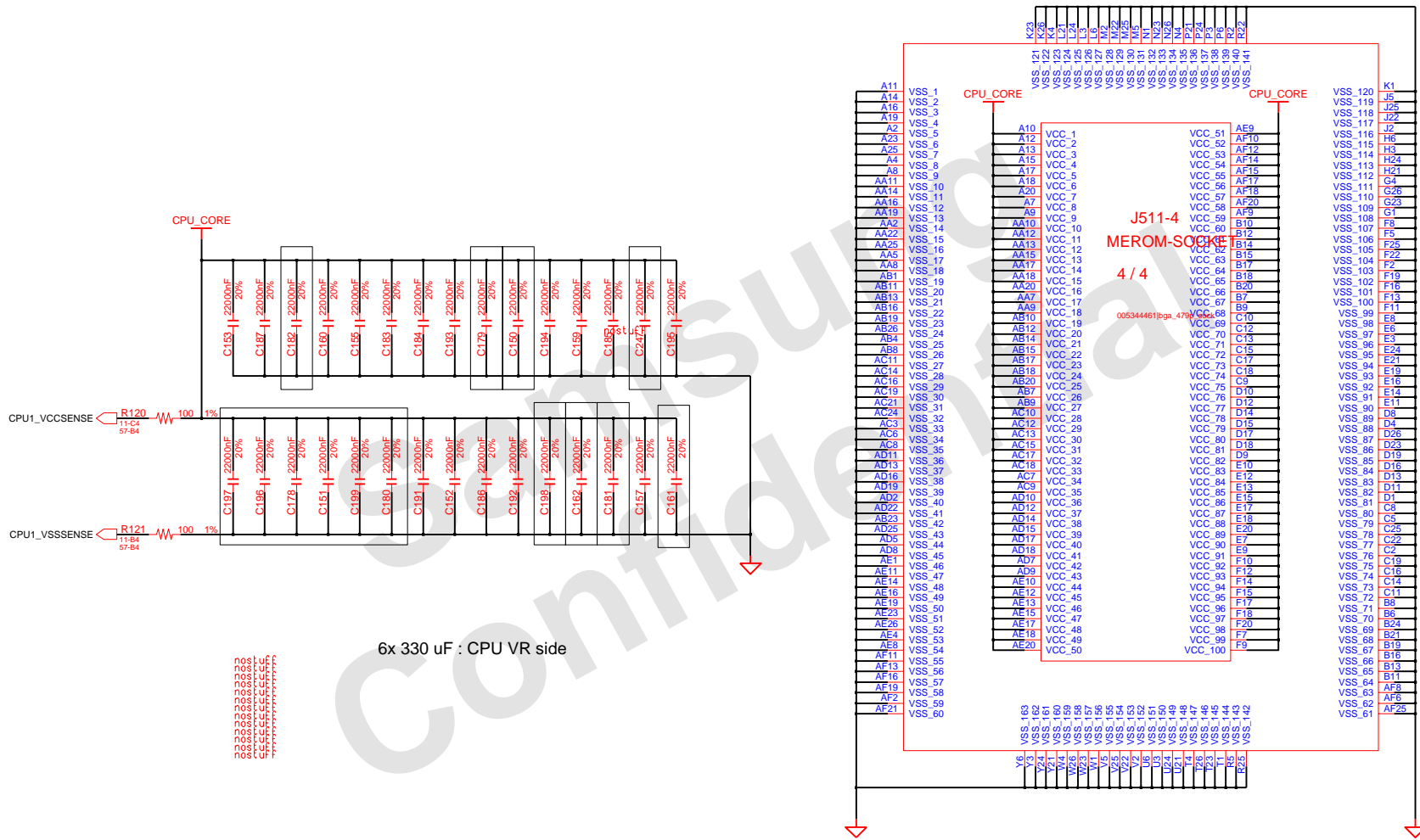
nostuff  
nostuff

IMVP-6

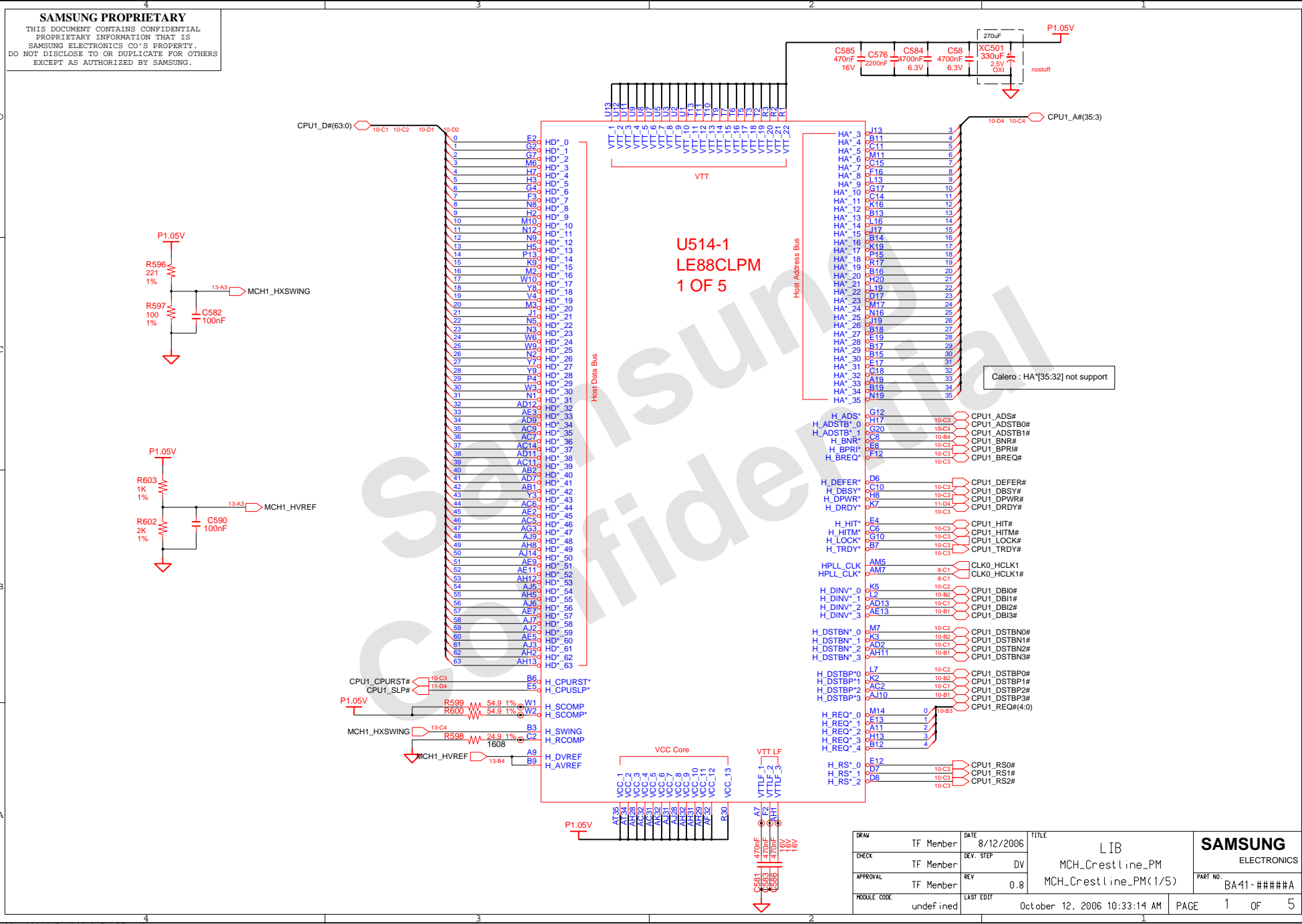
\*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a  $Z_0=55\text{ohm}$  traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

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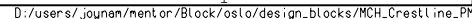


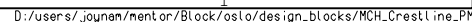
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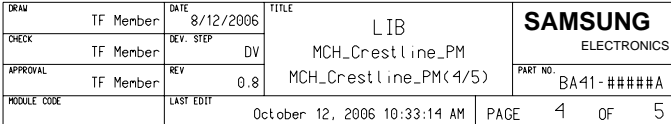
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APPROVAL	TF Member	REV	0.8	MCH_Crestline_PM(1/5)		
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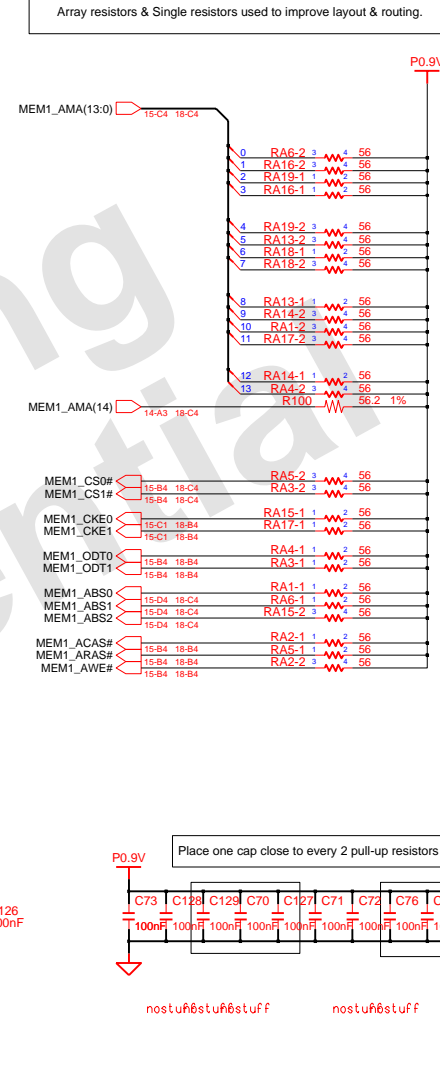
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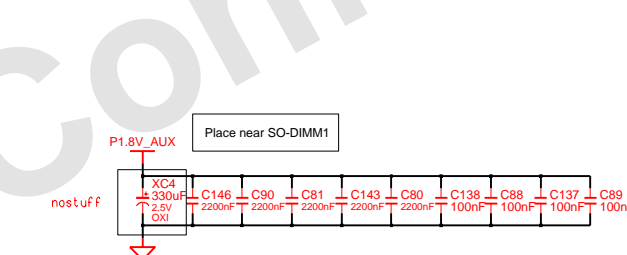
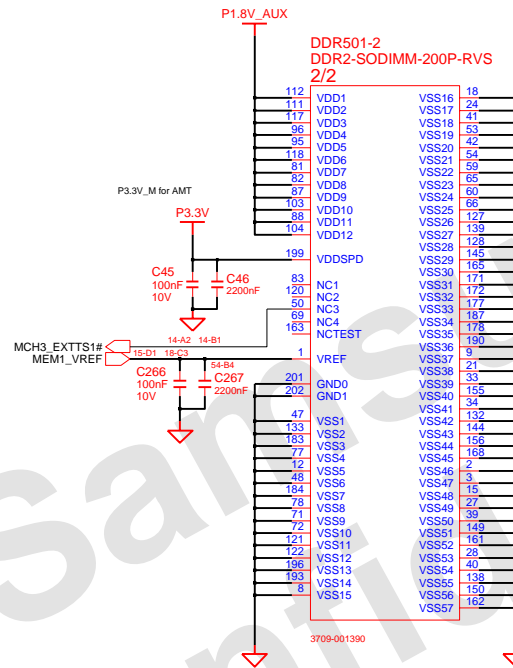
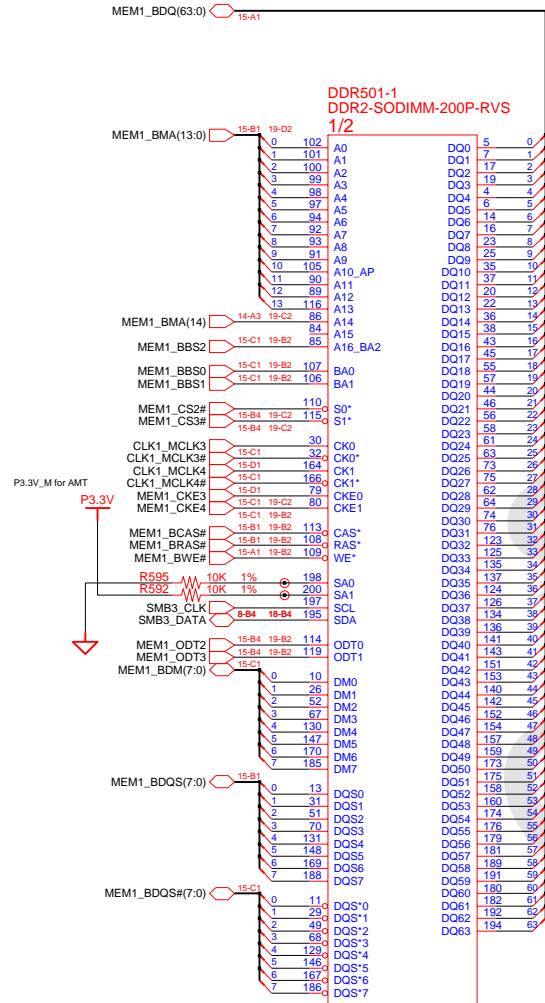


*POCAFEb-11 Only (Remove in MP Model)		
Current Setting (def. : default Option)		
CFG#	Low	High
CFG(5)	DMiX2	DMiX4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT	Dynamic ODT
	Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

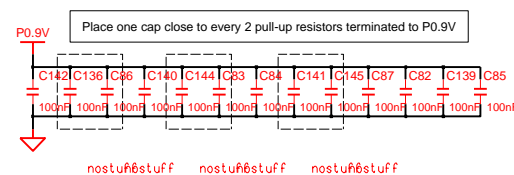
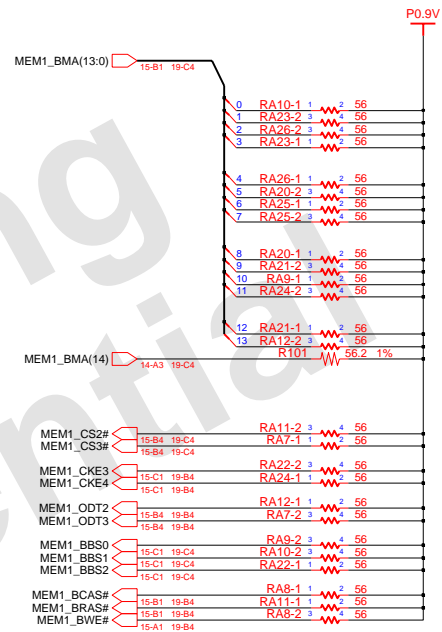


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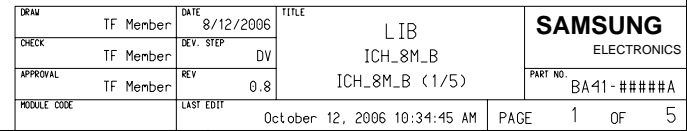
## DDR SO-DIMM #1



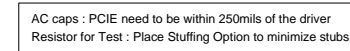
Array resistors & Single resistors used to improve layout & routing.



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV		SODIMM_DDR2	
APPROVAL	TF Member	REV	0.8		SODIMM_DDR2 #2	
MODULE CODE		LAST EDIT	October 10, 2006 20:55:25 PM	PAGE	2 OF 2	



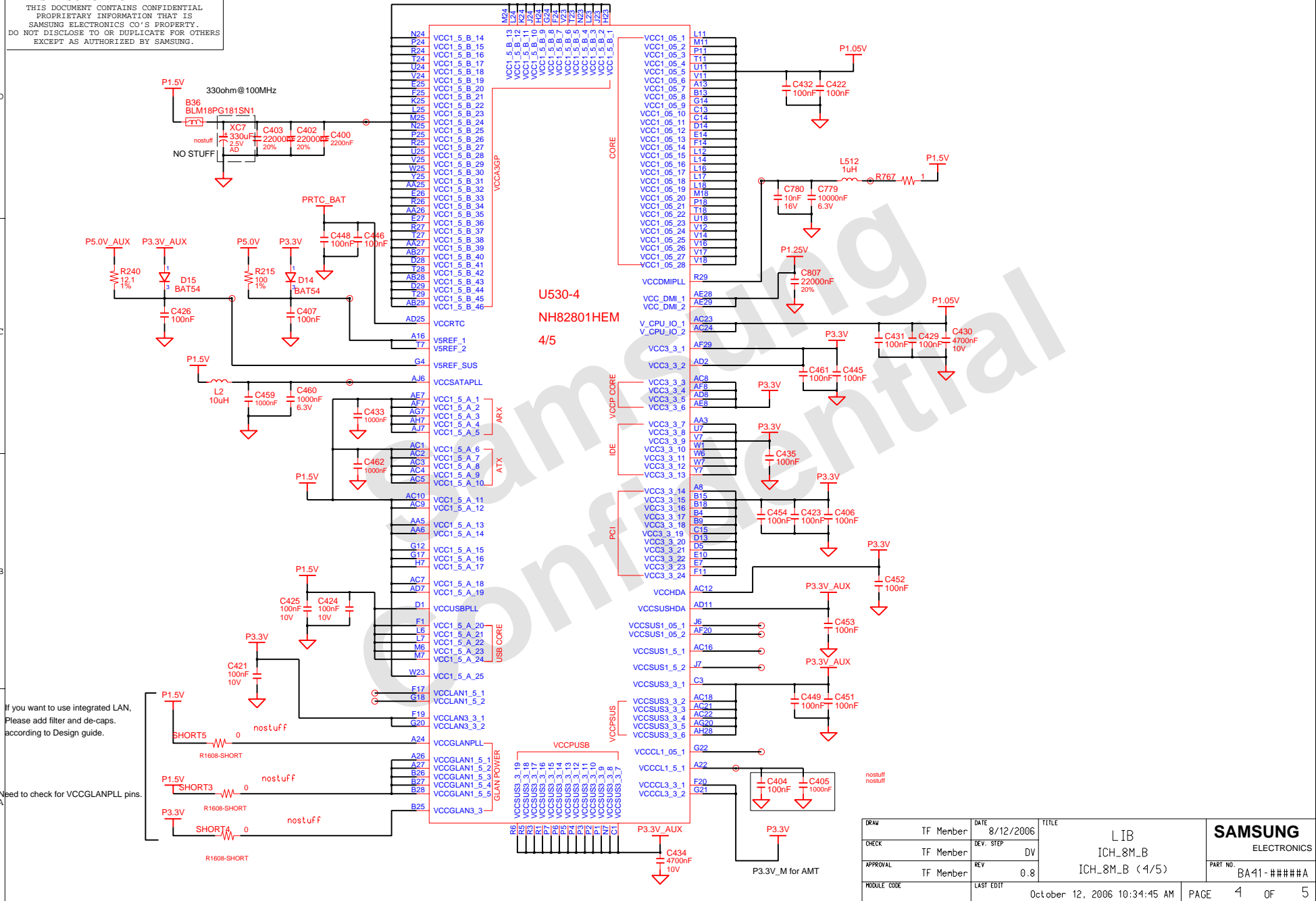
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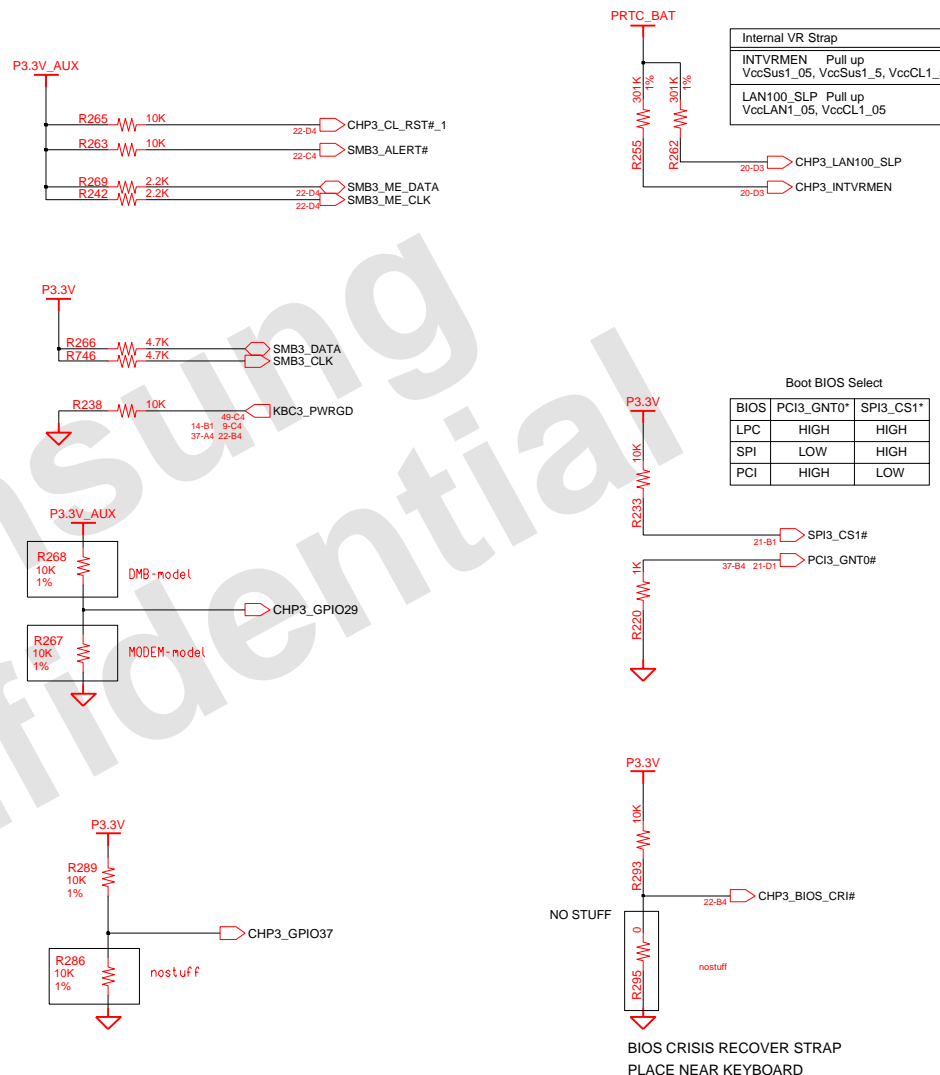
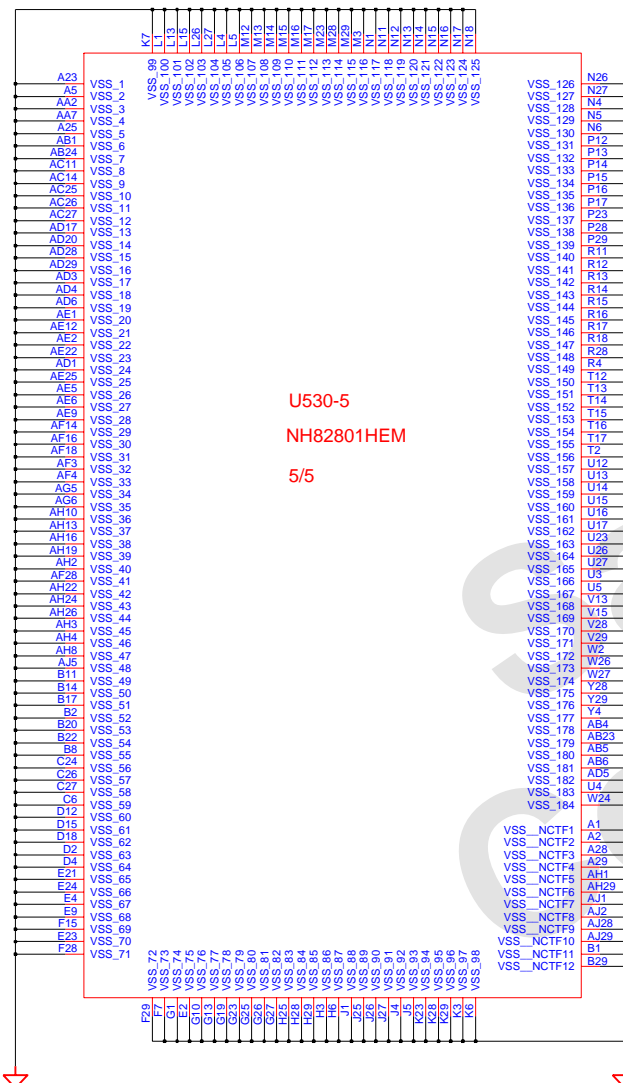
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CHECK	TF Member	DEV. STEP	DV						
APPROVAL	TF Member	REV	0.8						
MODULE CODE			LAST EDIT					October 12, 2006 10:34:45 AM	PAGE

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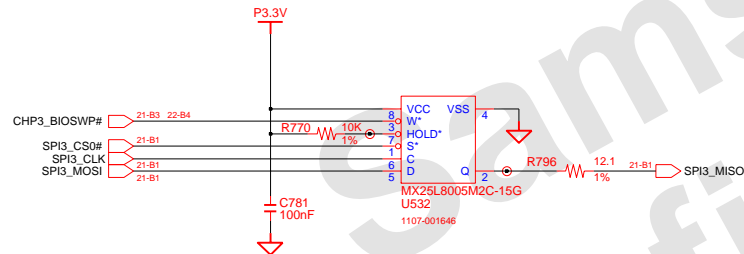


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## - SPI ROM LIST -

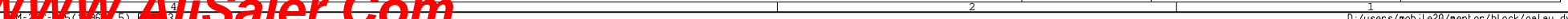
- Macronix - MX25L8005M2C-15G
  - STM - M25PE80
  - ATMEL - AT26DF081A-SU
- SST - 25VF080B-50-4C-S2AF  
WINBOND - W25X80-VSSI-G



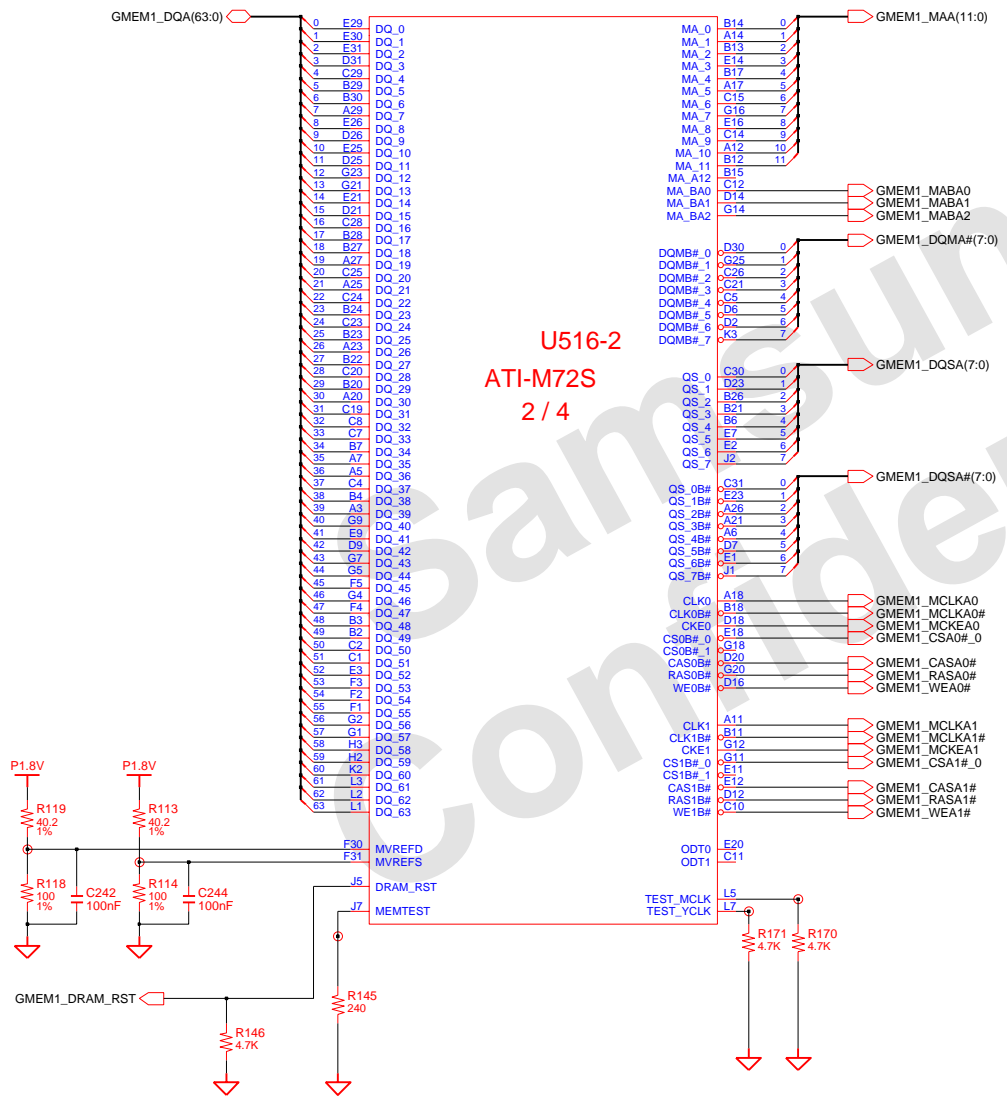
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPOMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY * PRESS ..... SETUP*	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV		SPI_BIOS_ROM	
APPROVAL	TF Member	REV	0.8		SPI_BIOS_ROM	
MODULE CODE		LAST EDIT				
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	C
	V
	P

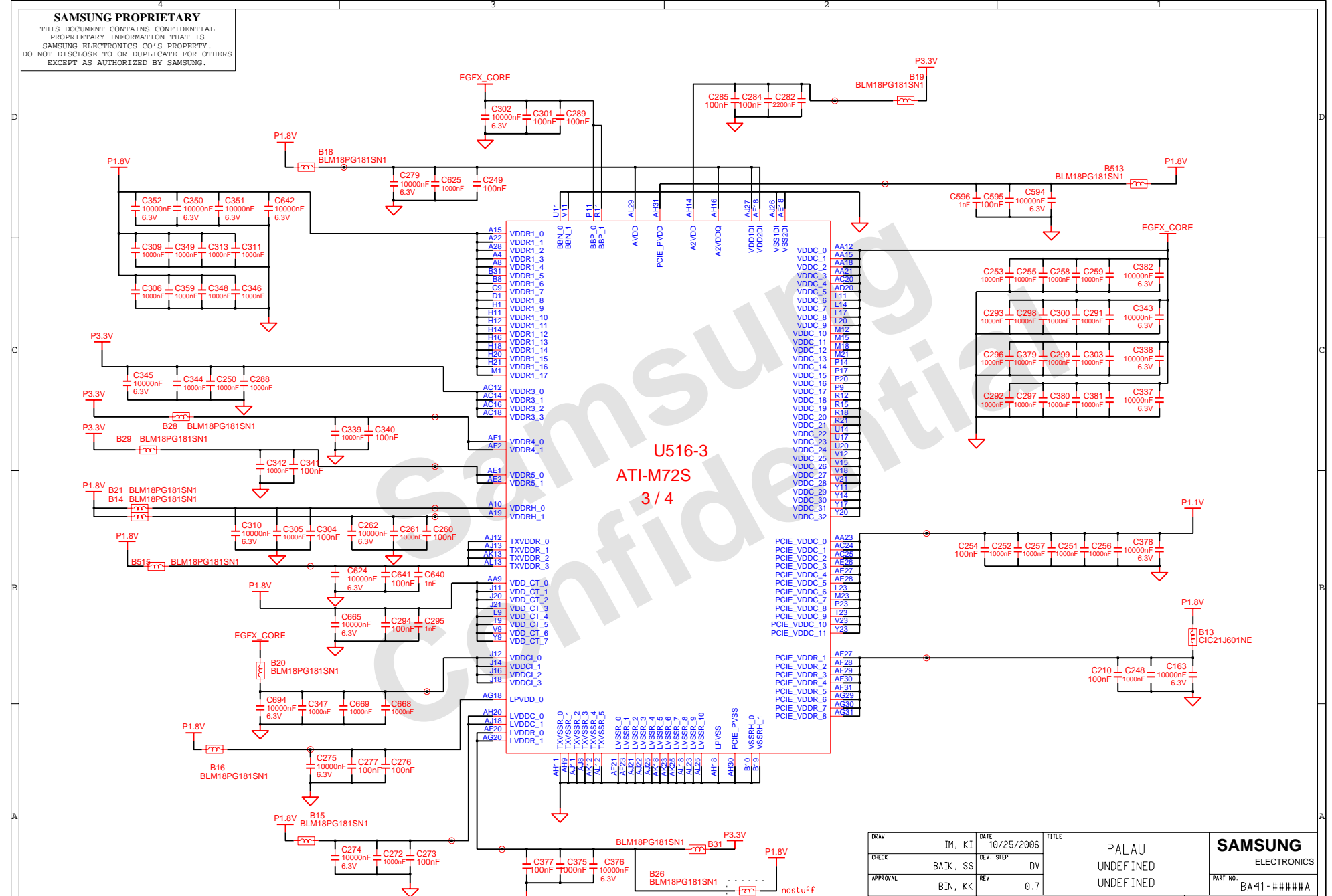


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DRAW	IM, KI	DATE	10/25/2006	TITLE	PALAU UNDEFINED	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	REV	0.7	
APPROVAL	BIN, KK	LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	17	OF 22
MODULE CODE						

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CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	0.7			
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	18 OF 22	

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D

C

B

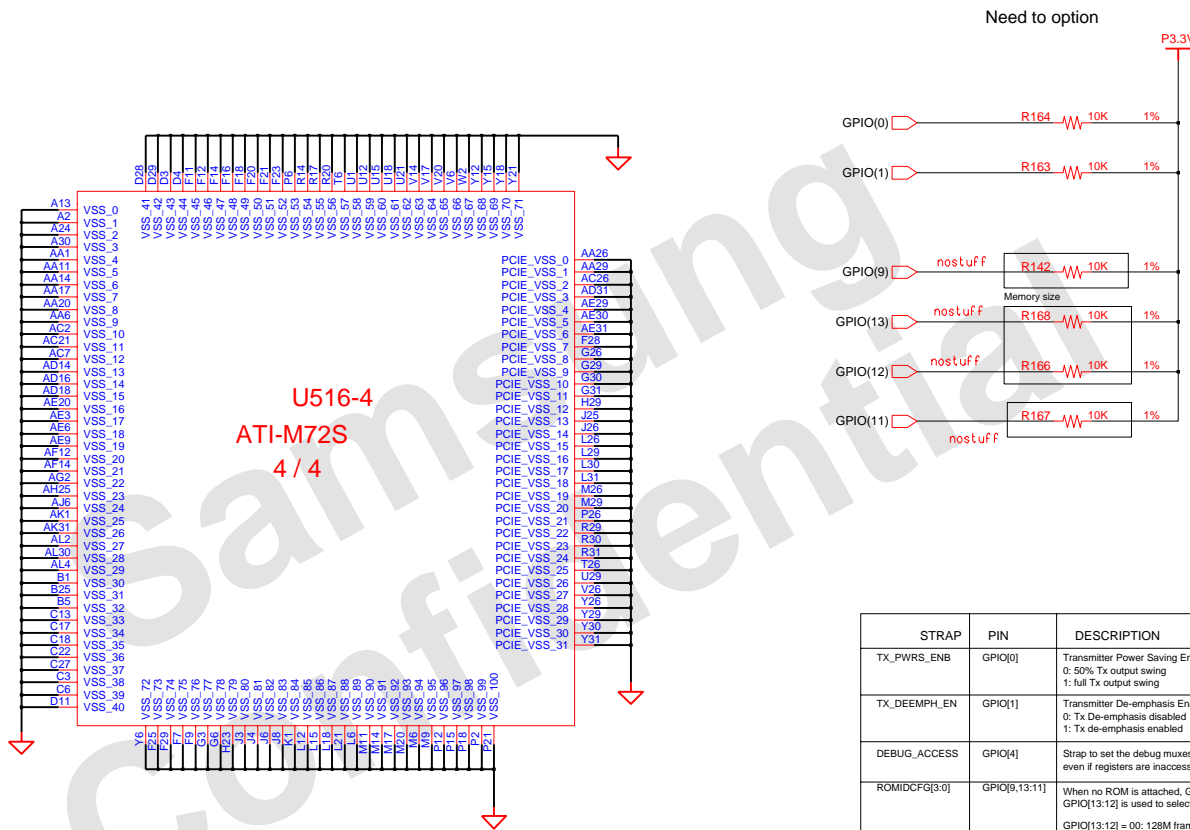
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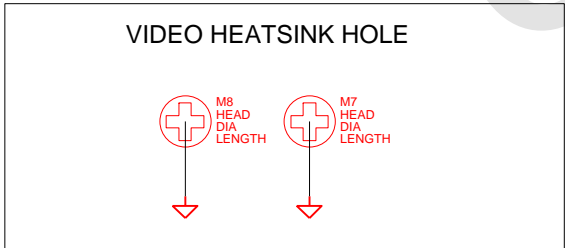
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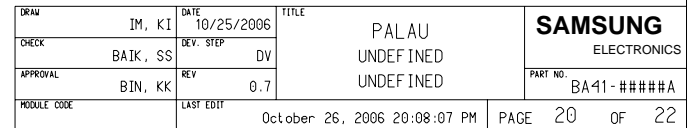
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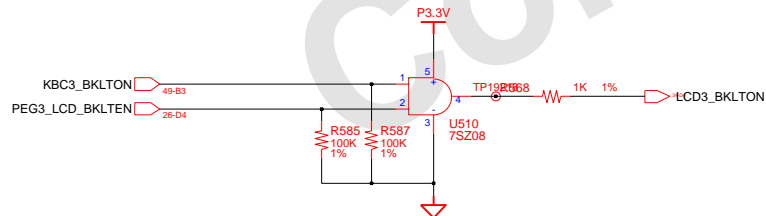
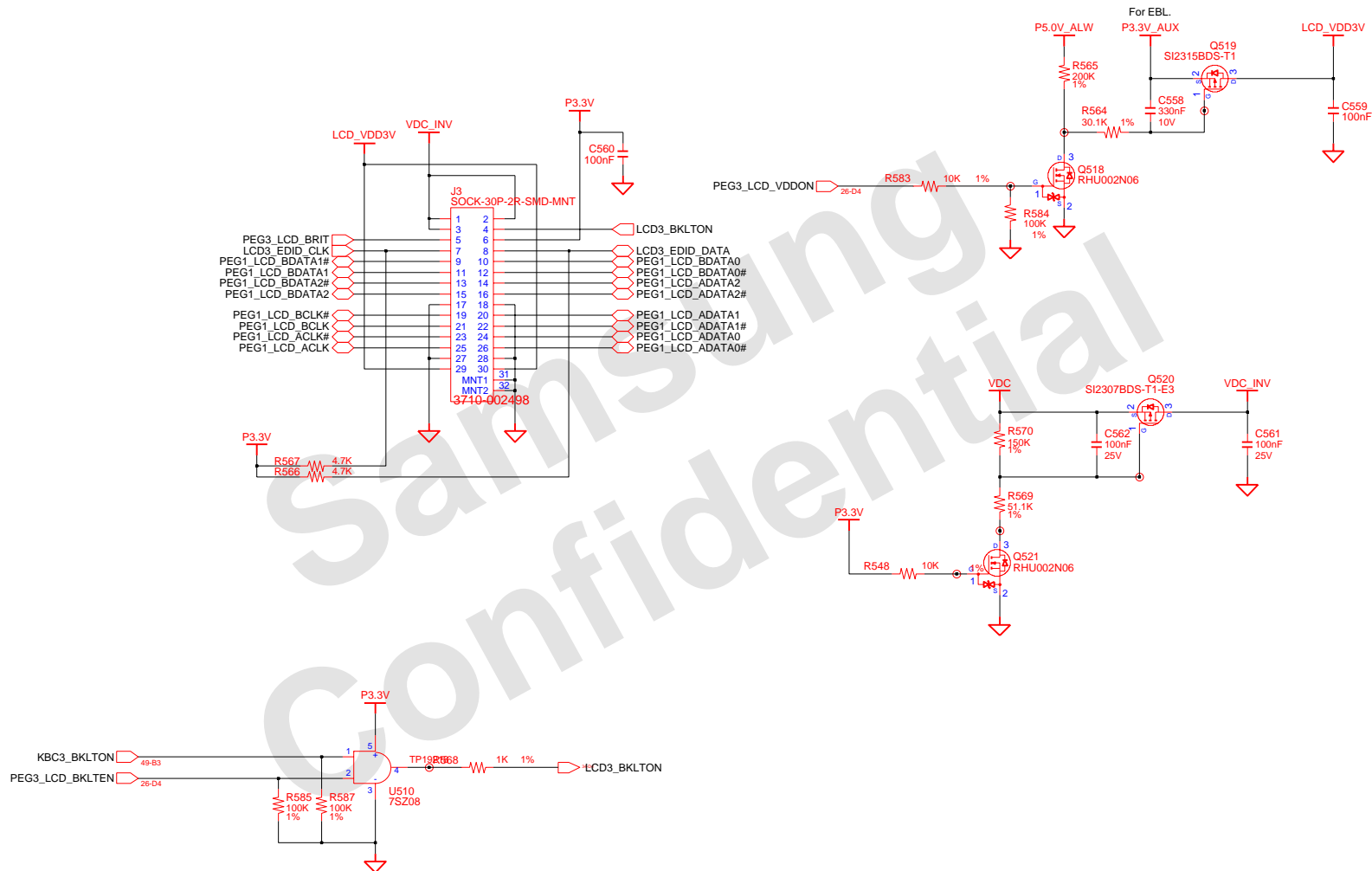


(DEFAULT : pull-down)		
STRAP	PIN	DESCRIPTION
TX_PWRS_ENB	GPIO[0]	Transmitter Power Saving Enable 0: 50% Tx output swing 1: full Tx output swing
TX_DEEMPH_EN	GPIO[1]	Transmitter De-emphasis Enable 0: Tx De-emphasis disabled 1: Tx de-emphasis enabled
DEBUG_ACCESS	GPIO[4]	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.
ROMIDCFG[3:0]	GPIO[9,13:11]	When no ROM is attached, GPIO[9] is set to 0. GPIO[13:12] is used to select the frame buffer aperture size.  GPIO[13:12] = 00: 128M frame buffer GPIO[13:12] = 01: 256M frame buffer GPIO[13:12] = 10: 64M frame buffer GPIO[13:12] = 11: reserved



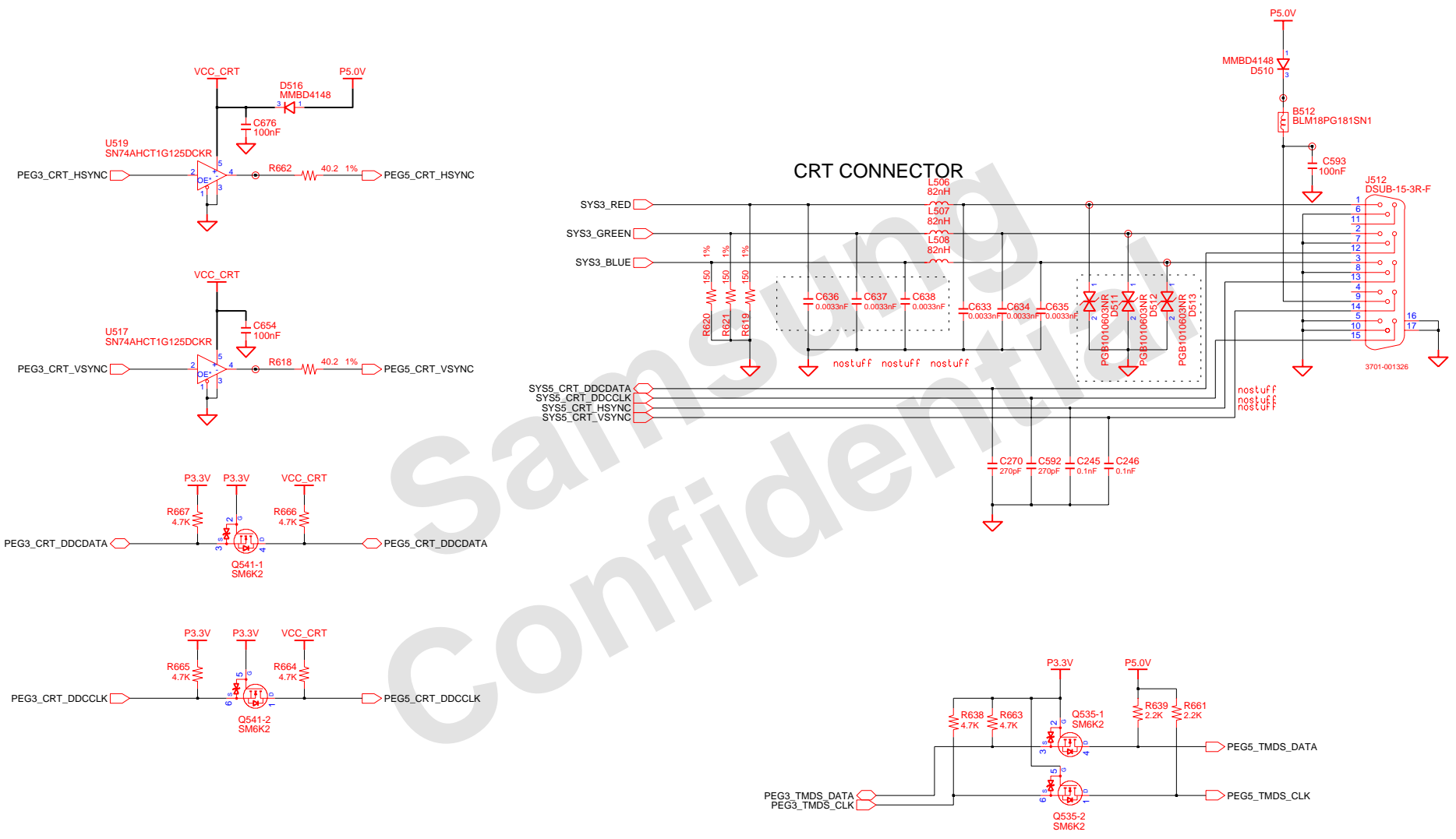
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CHECK	BAIK, SS	DEV. STEP	DV		UNDEFINED	ELECTRONICS
APPROVAL	BIN, KK	REV	0.7		UNDEFINED	PART NO.
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	19	BA41-####A
				OF	22	





DEW	TF Member	DATE	8/12/2006	TITLE	LIB	<b>SAMSUNG</b> ELECTRONICS	
CHECK	TF Member	DEV. STEP	DV				LCD_IF_14p1
APPROVAL	TF Member	REV	0.8				LCD_IF_14p1
				PART NO.	BA41-#####		
MODULE CODE	undef:ined	LAST EDIT			October 10, 2006 20:42:58 PM	PAGE 1 OF 1	

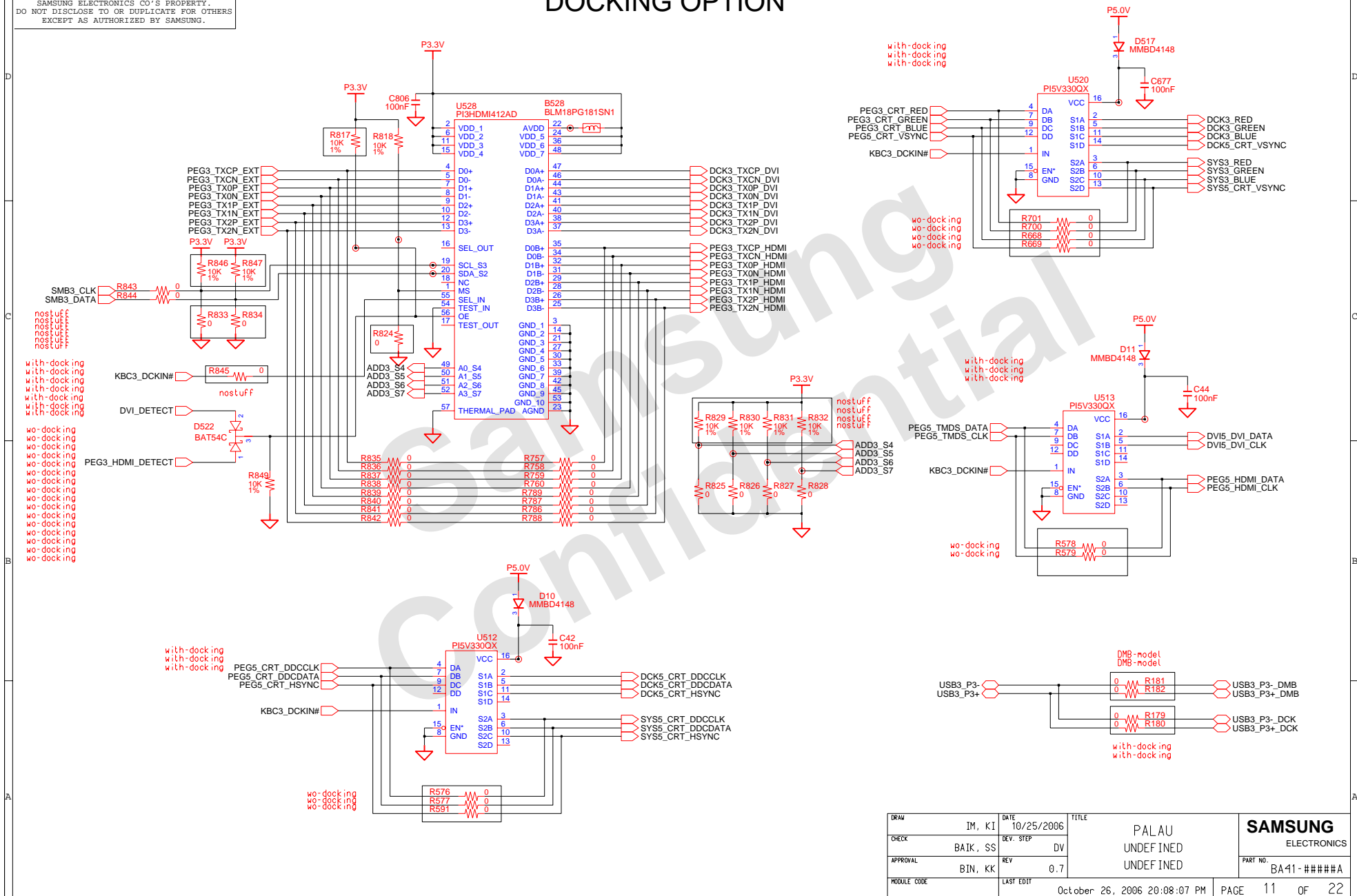
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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB Interface_Circuit Graphics_IF_CRT	<b>SAMSUNG</b> ELECTRONICS
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MODULE CODE				LAST EDIT	October 10, 2006 20:30:38 PM	PART NO. BA41-####A
					PAGE 1	OF 1

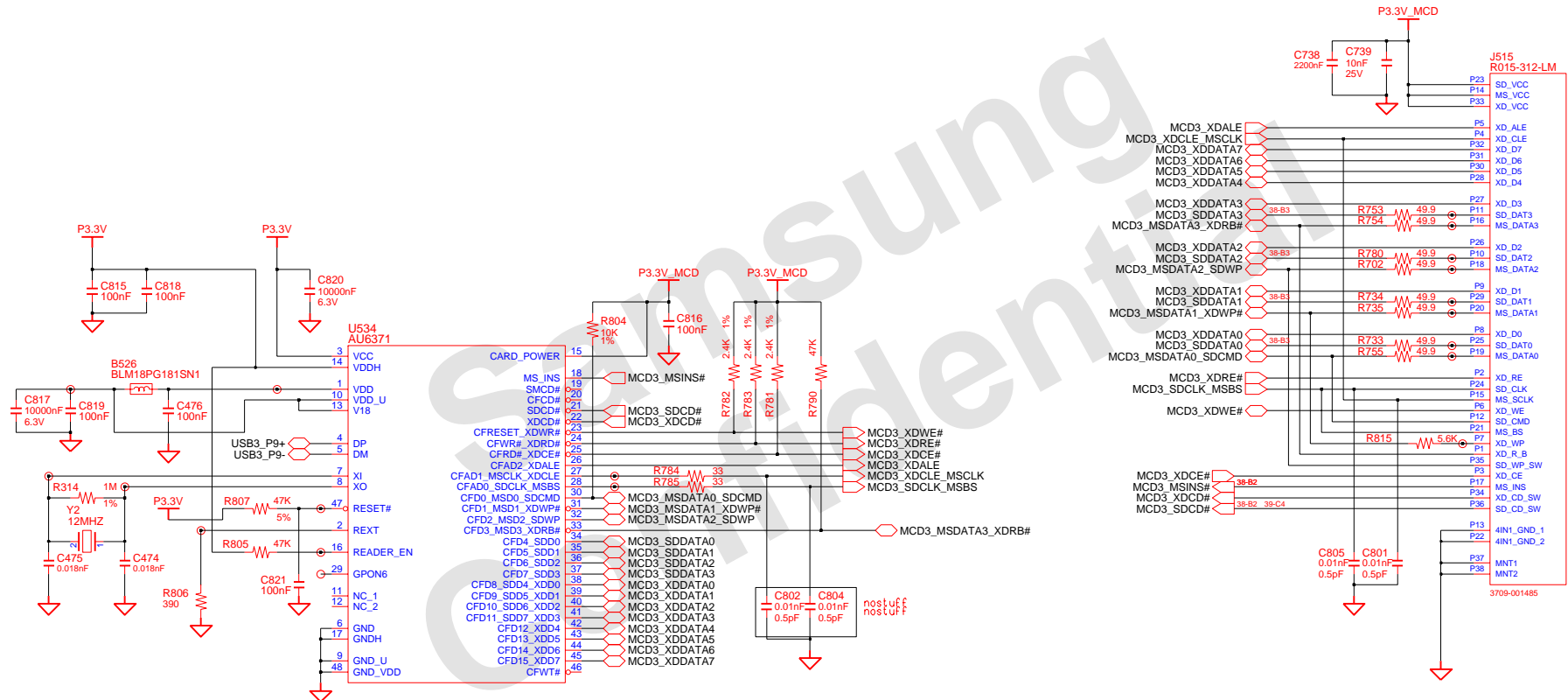


## DOCKING OPTION



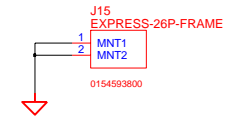
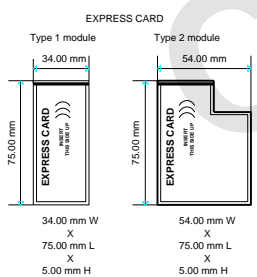
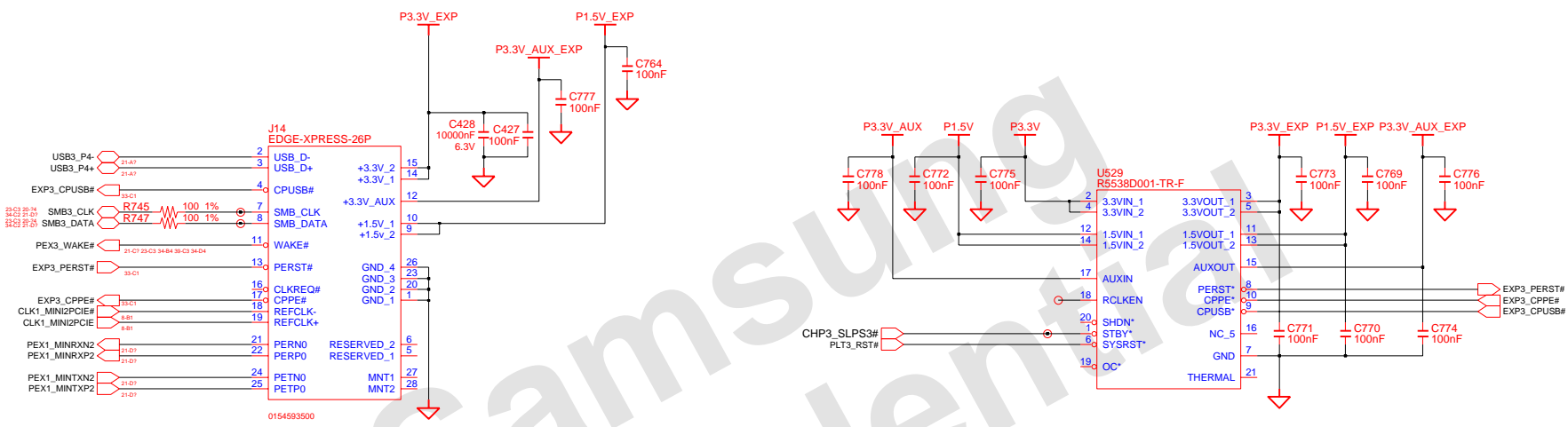
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CHECK	BAIK, SS	DEV. STEP	DV			PART NO. BA41-####A
APPROVAL	BIN, KK	REV	0.7			
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	11 OF 22	

# MEMORY CARD CONTROLLER



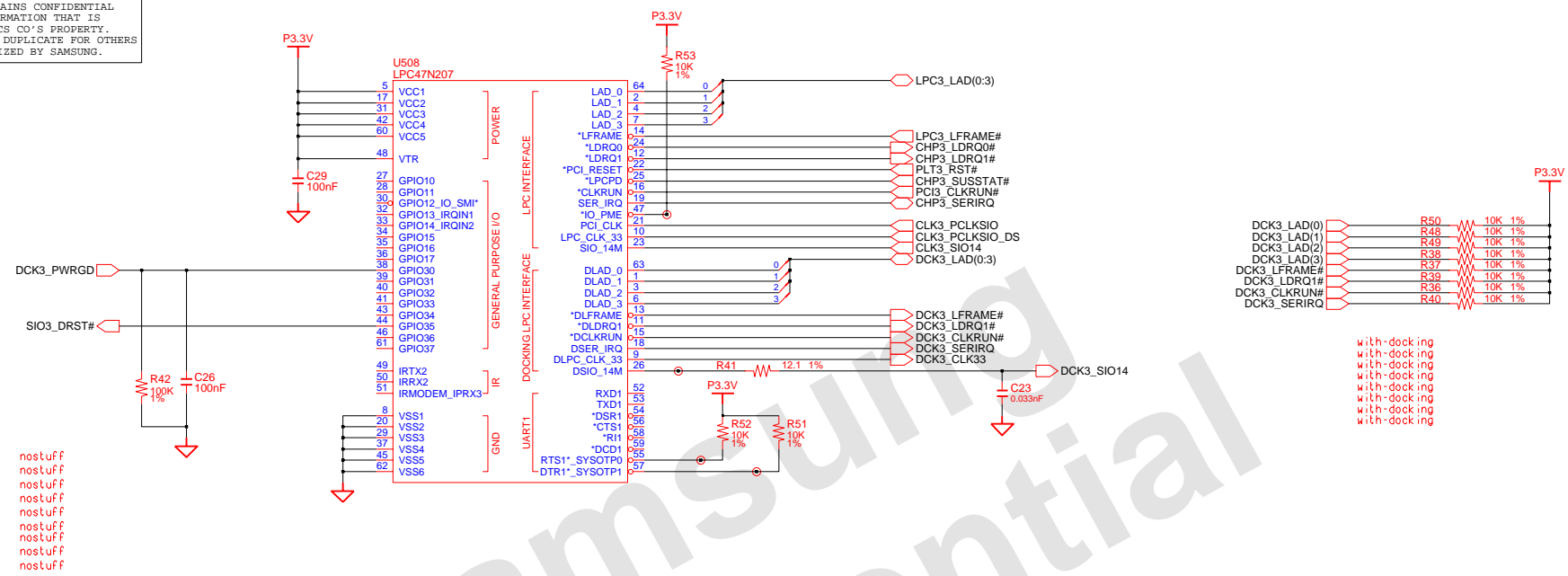
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CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	0.7			
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	12 OF 22	

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DRAW	IM, KI	DATE	10/25/2006	TITLE	PALAU UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	0.7			
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	13	OF 22

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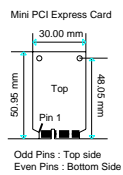
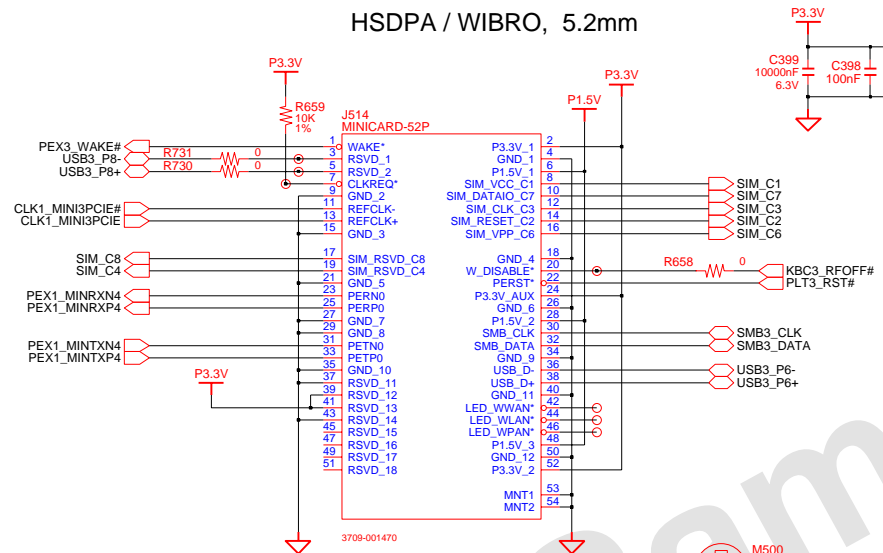
nostuff  
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with-docking  
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with-docking

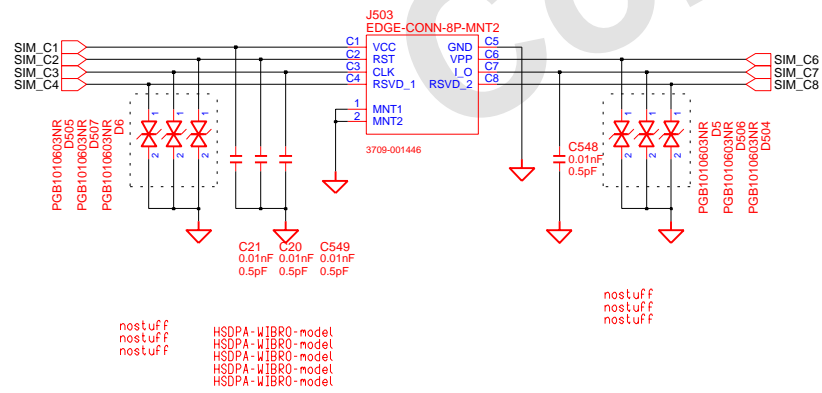
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CHECK	BAIK, SS	DEV. STEP	DV			PART NO. BA41-####A
APPROVAL	BIN, KK	REV	0.7			
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	14 OF 22	

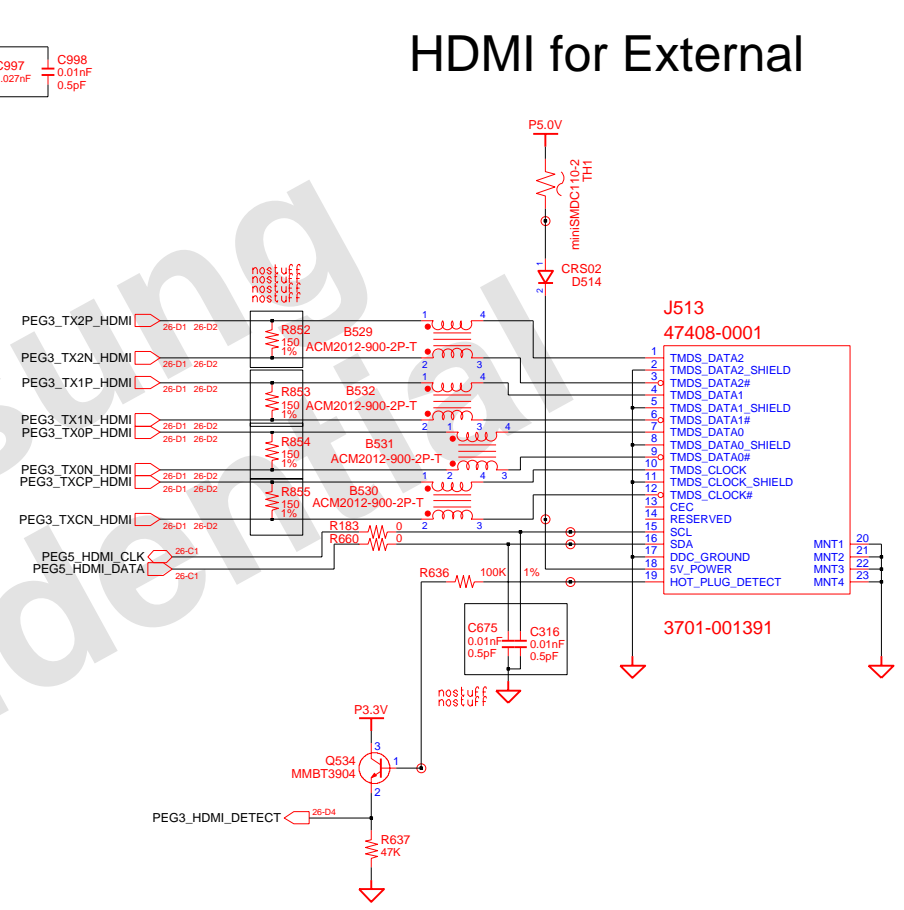
HSDPA / WIBRO, 5.2mm



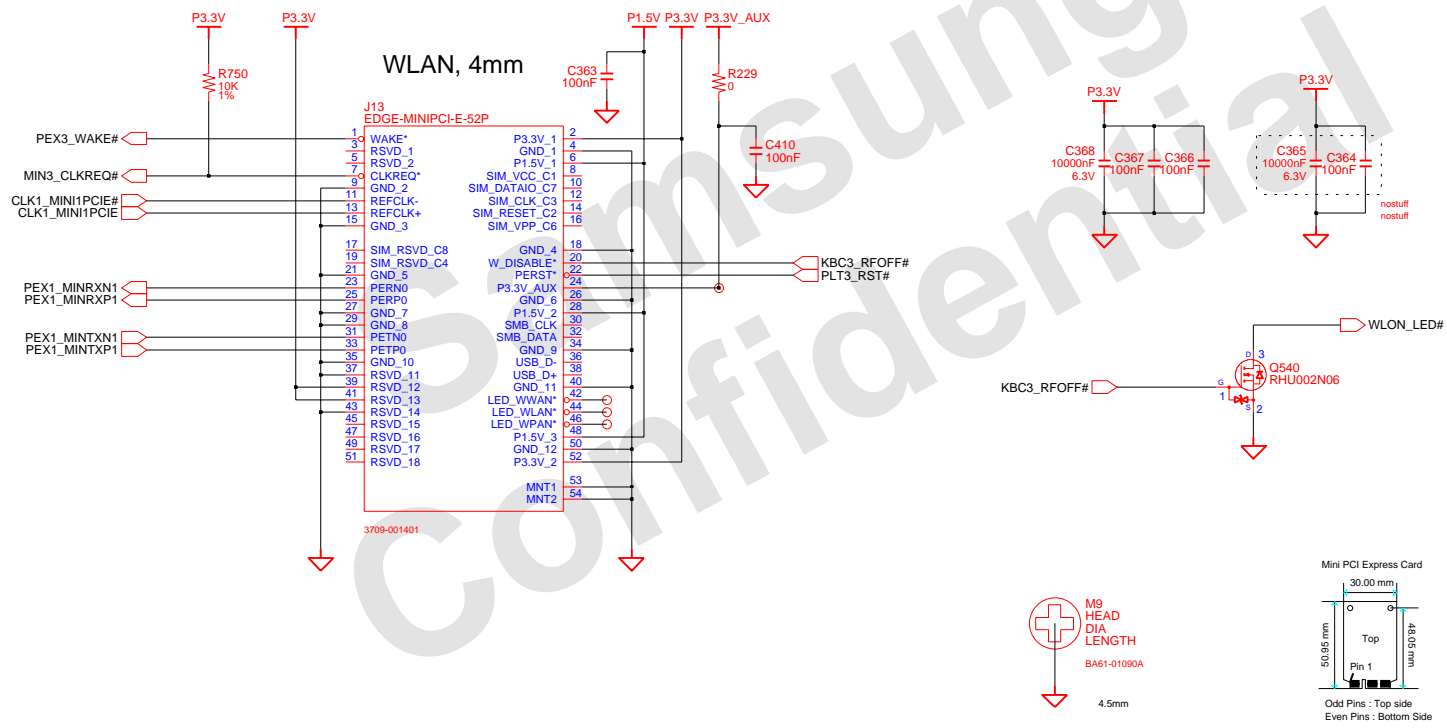
SIM CARD CONN.



HDMI for External

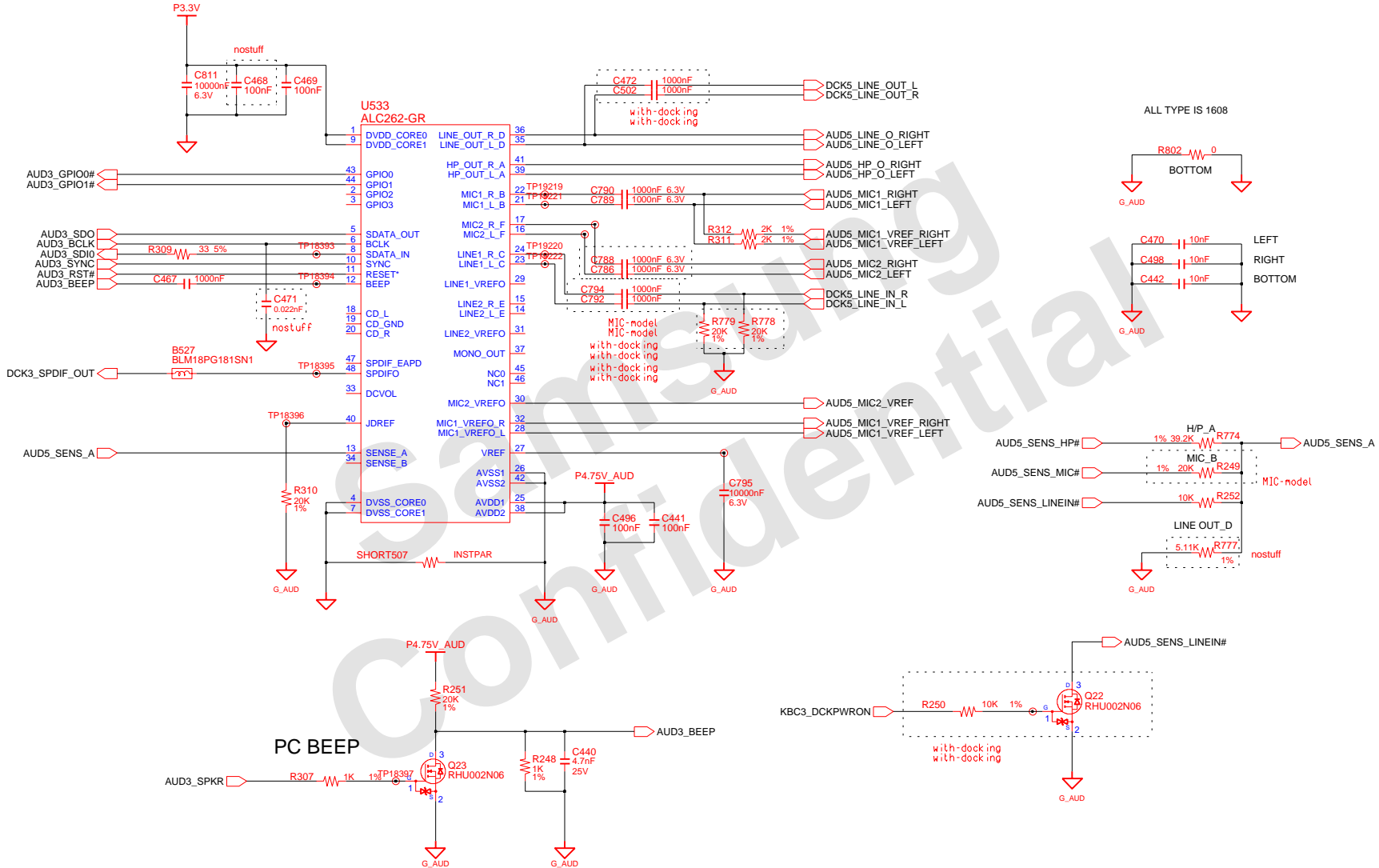


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MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM			BA41-####A
					PAGE	15 OF 22



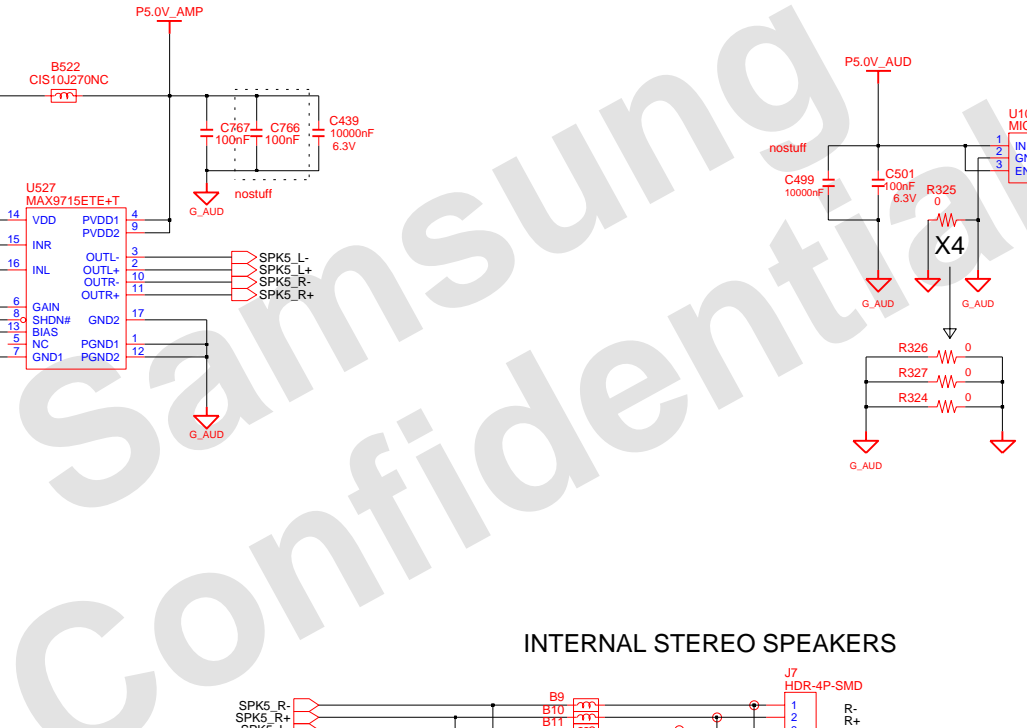
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APPROVAL	TF Member	REV	0.8	PCIE_Minicard_Slot		
MODULE CODE	undefined	LAST EDIT	October 10, 2006 20:46:07 PM	PAGE	1 OF 1	

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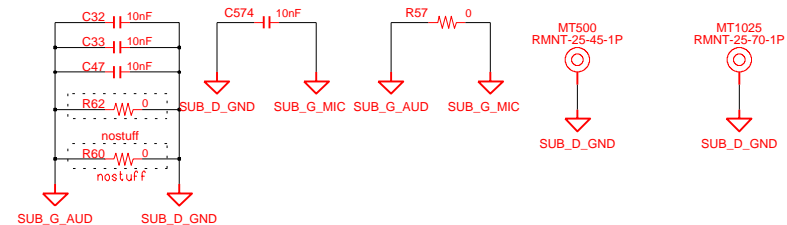
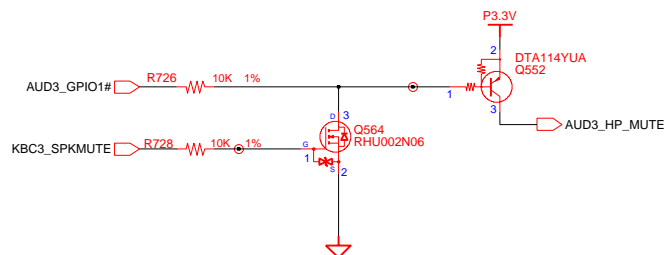
**Test**

**Test**

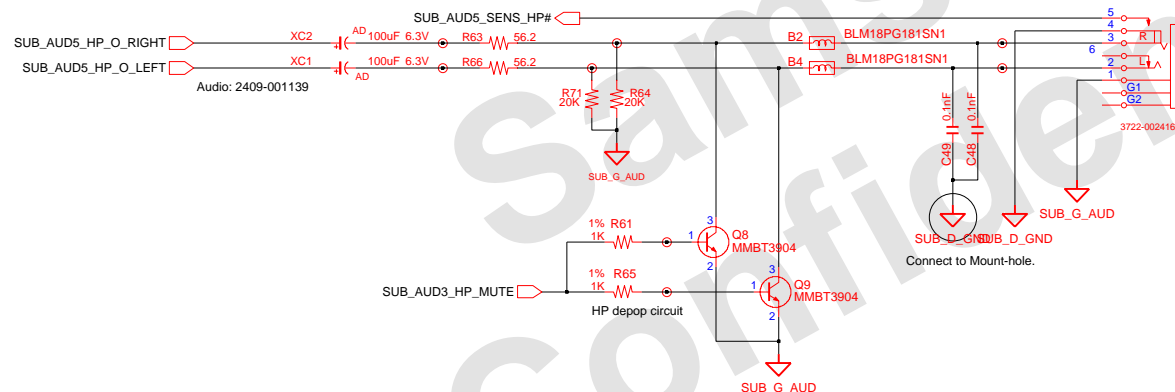




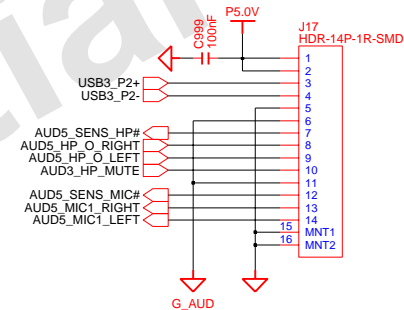




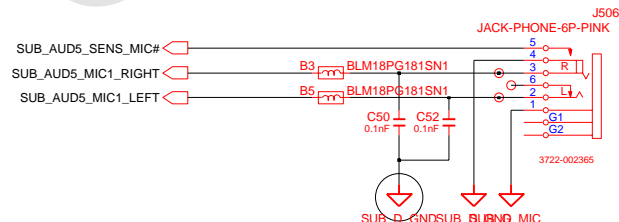
## HEADPHONE



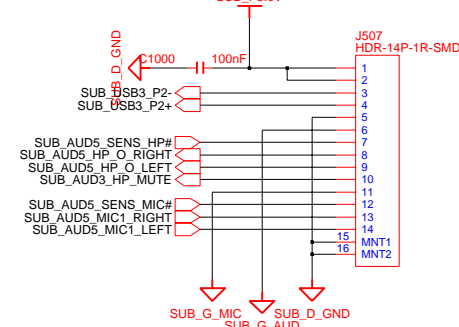
## MAIN BOARD SIDE



## MIC JACK



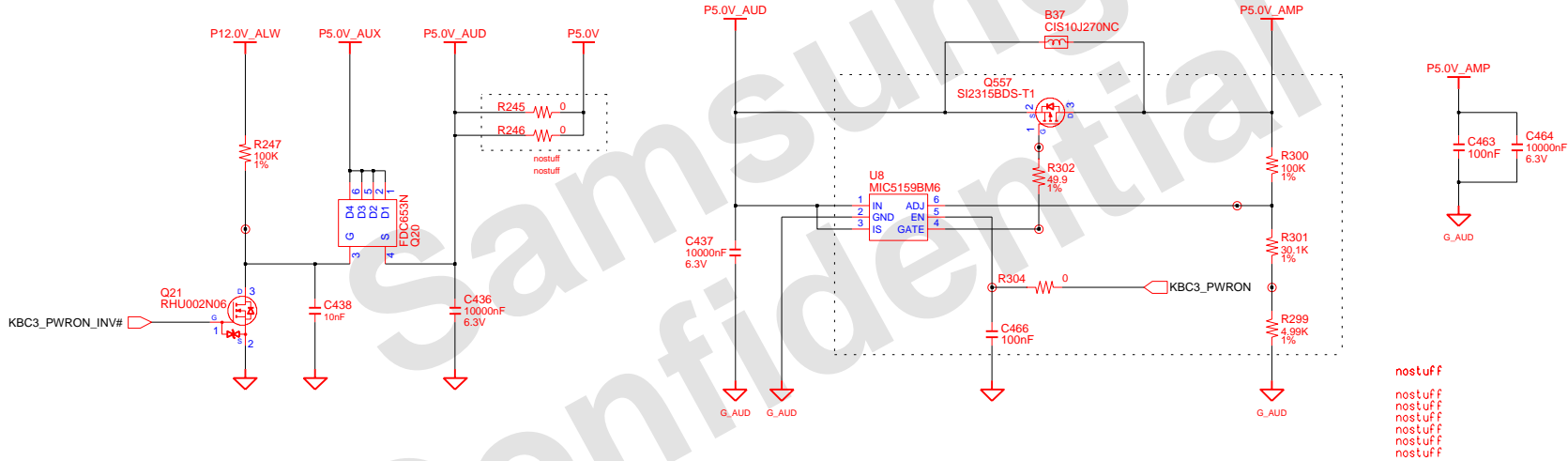
## SUB BOARD SIDE



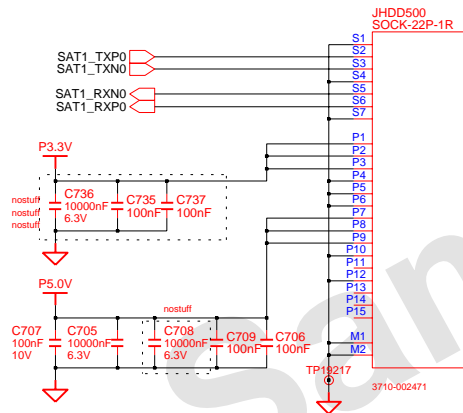
The traces led to Audio Jacks have the width over 10mil

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	HDA_Codec_Alc262		
APPROVAL	TF Member	REV	0.8	HDA_Codec_Alc262 #4		
MODULE CODE		LAST EDIT	October 10, 2006 20:35:33 PM	PAGE	4 OF 5	

# AUDIO POWER



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	HDA_Codec_Alc262		
APPROVAL	TF Member	REV	0.8	HDA_Codec_Alc262 #5	PART NO.	
MODULE CODE	undefined	LAST EDIT	October 10, 2006 20:35:33 PM	PAGE	5 OF 5	

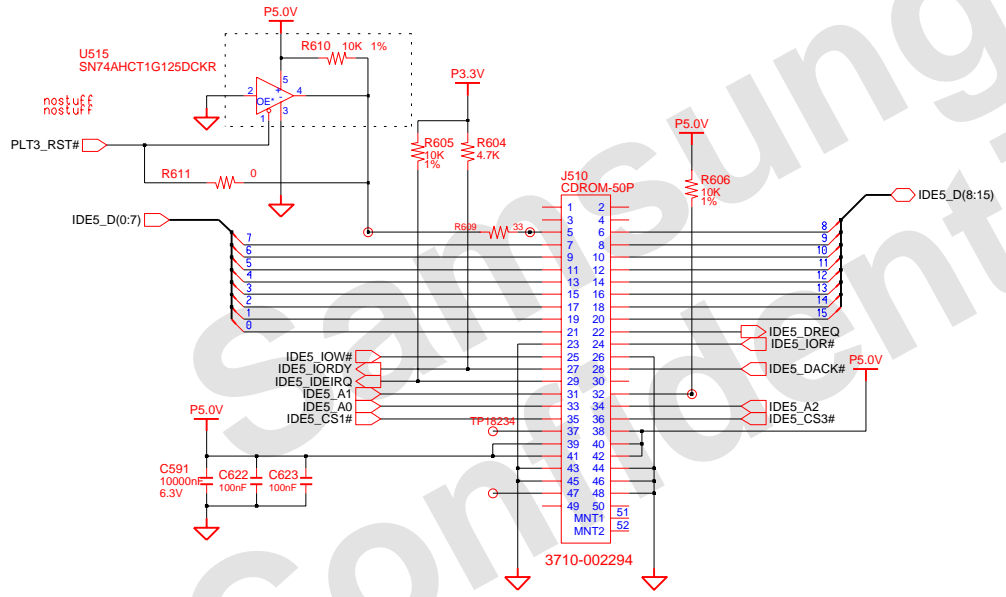


	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Master)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Slave)

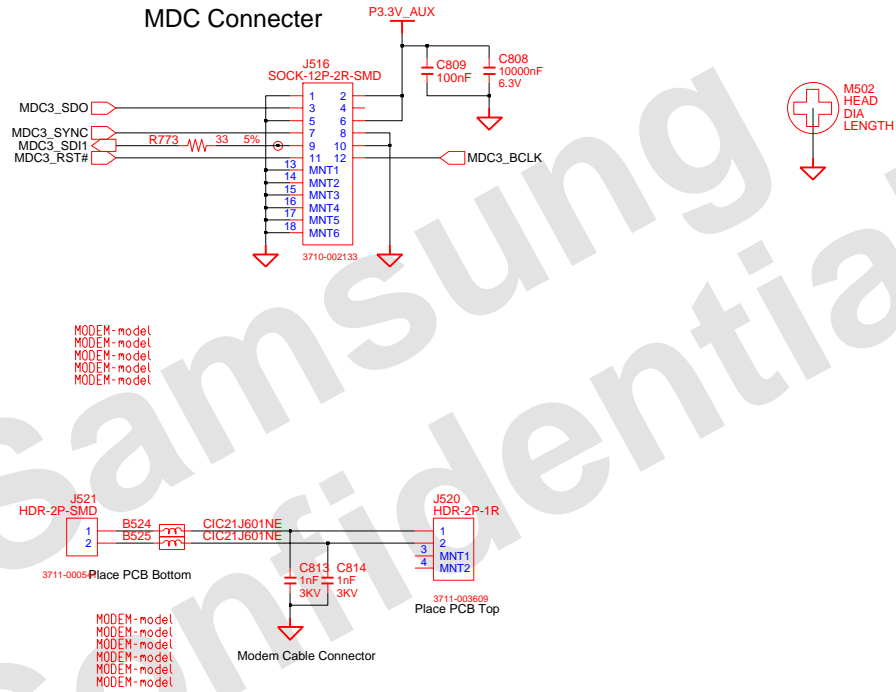
DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV		HDD_IF_Conn	
APPROVAL	TF Member	REV	0.8		HDD_IF_Conn	
MODULE CODE		LAST EDIT	October 12, 2006 12:18:59 PM	PAGE	1 OF 1	

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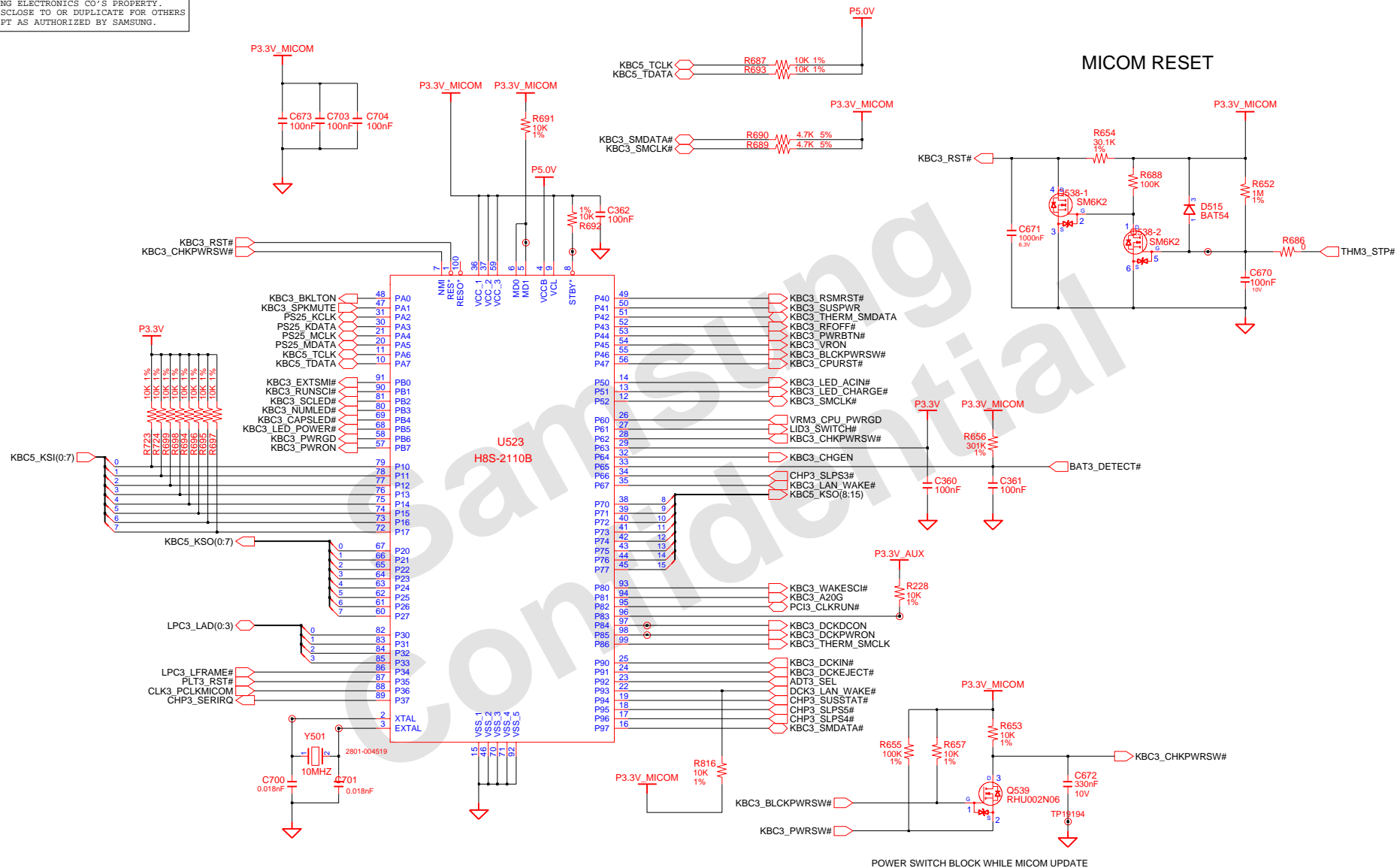
	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Master)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Slave)



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	ODD_IF_Conn	ODD_IF_Conn	
APPROVAL	TF Member	REV	0.8			
MODULE CODE		LAST EDIT	October 12, 2006 12:19:50 PM	PAGE	1 OF 1	

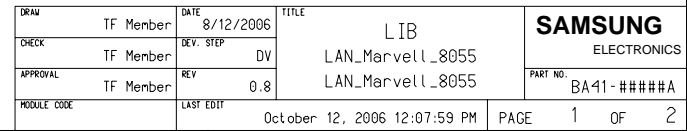


DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
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APPROVAL	TF Member	REV	0.8		HDA_Modem	
MODULE CODE		LAST EDIT	October 10, 2006 20:37:02 PM	PAGE	1 OF 1	



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	MICOM_Renesas2110_100p		
APPROVAL	TF Member	REV	0.8	MICOM_Renesas2110_100p		
MODULE CODE		LAST EDIT	October 12, 2006 11:48:20 AM	PAGE	1 OF 1	

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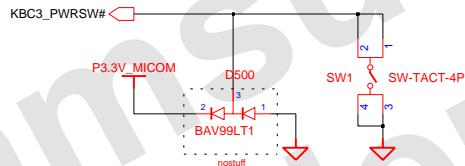
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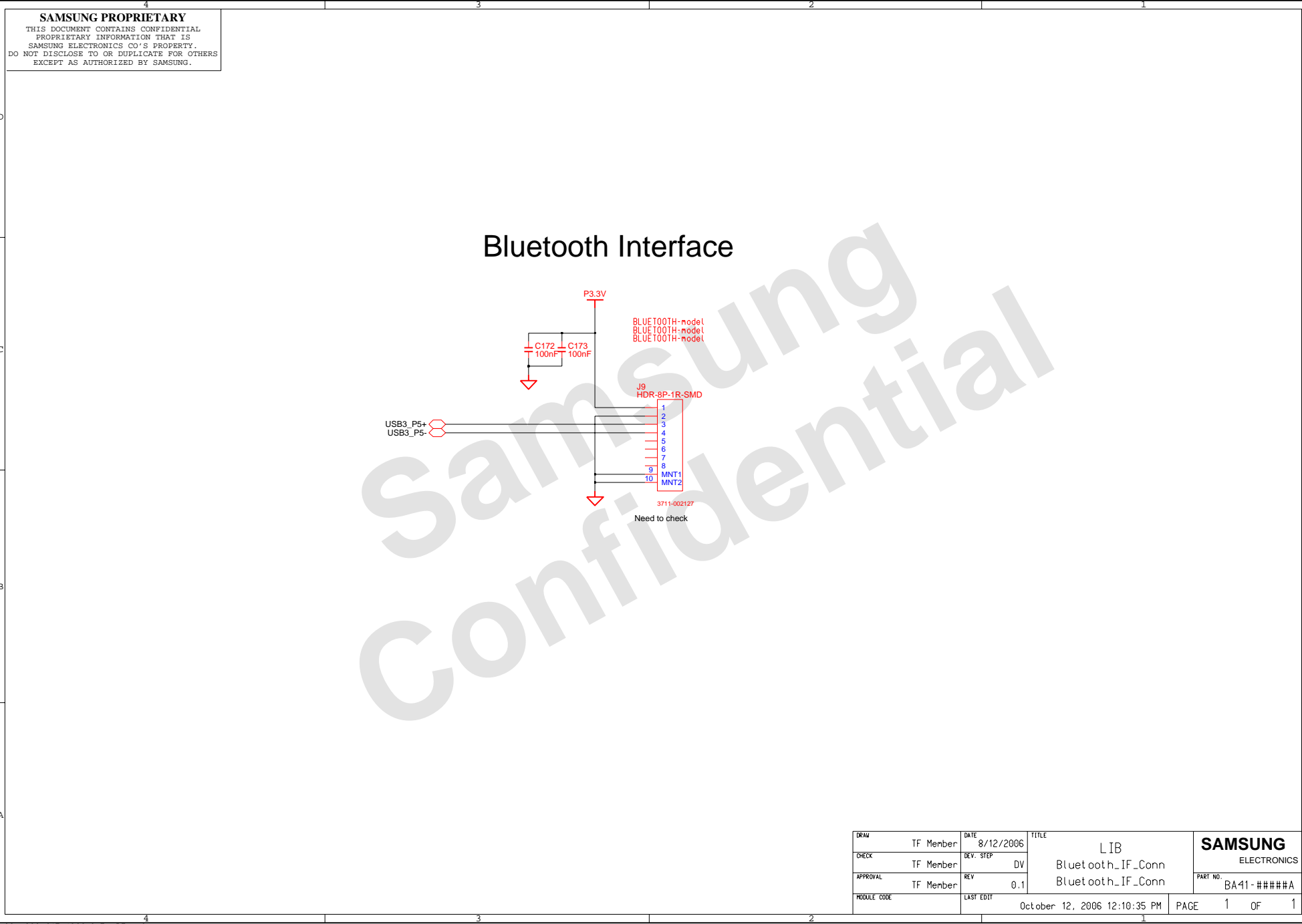
Place near to the Marvell chip.

DRAW	TF Member	DATE	8/12/2006	LIB LAN_Marvell_8055 LAN_Marvell_8055	SAMSUNG ELECTRONICS		
CHECK	TF Member	DEV. STEP	DV				
APPROVAL	TF Member	REV	0.8		PART NO.	BA41-#####	
MODULE CODE	LAST EDIT				October 12, 2006 12:07:59 PM	PAGE	2 OF 2

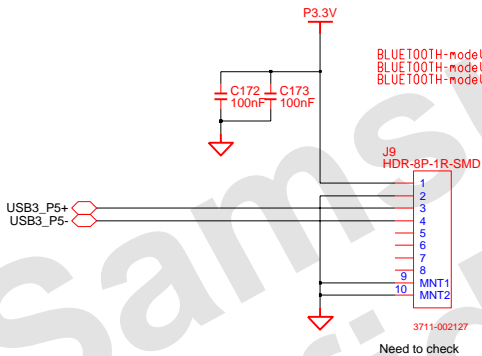
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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	PWR_Switchbutton	PART NO.	
APPROVAL	TF Member	REV	0.8	PWR_Switchbutton	BA41-####A	
MODULE CODE	LAST EDIT			October 10, 2006 20:53:26 PM	PAGE	1 OF 1



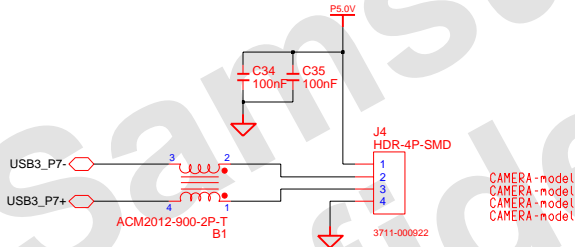
Bluetooth Interface



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	Bluetooth_IF_Conn		
APPROVAL	TF Member	REV	0.1	Bluetooth_IF_Conn		
MODULE CODE		LAST EDIT	October 12, 2006 12:10:35 PM	PAGE	1	OF 1

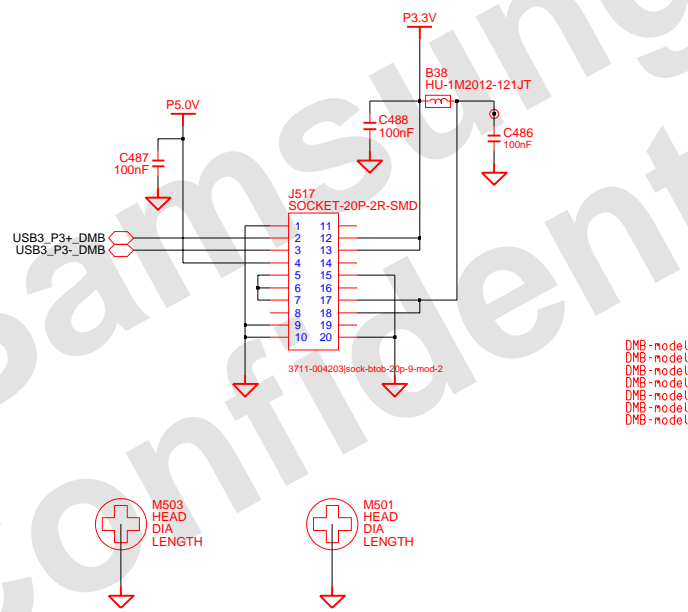
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CAMERA



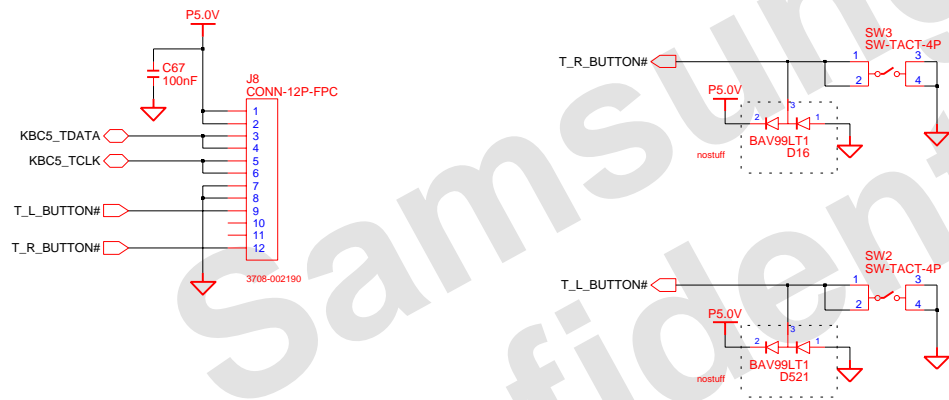
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CHECK	TF Member	DEV. STEP	DV	Camera_IF_Conn	Camera_IF_Conn	ELECTRONICS
APPROVAL	TF Member	REV	0.8	Camera_IF_Conn	Camera_IF_Conn	PART NO. BA41-####A
MODULE CODE		LAST EDIT	October 12, 2006 12:13:19 PM	PAGE	1	OF 1

DMB

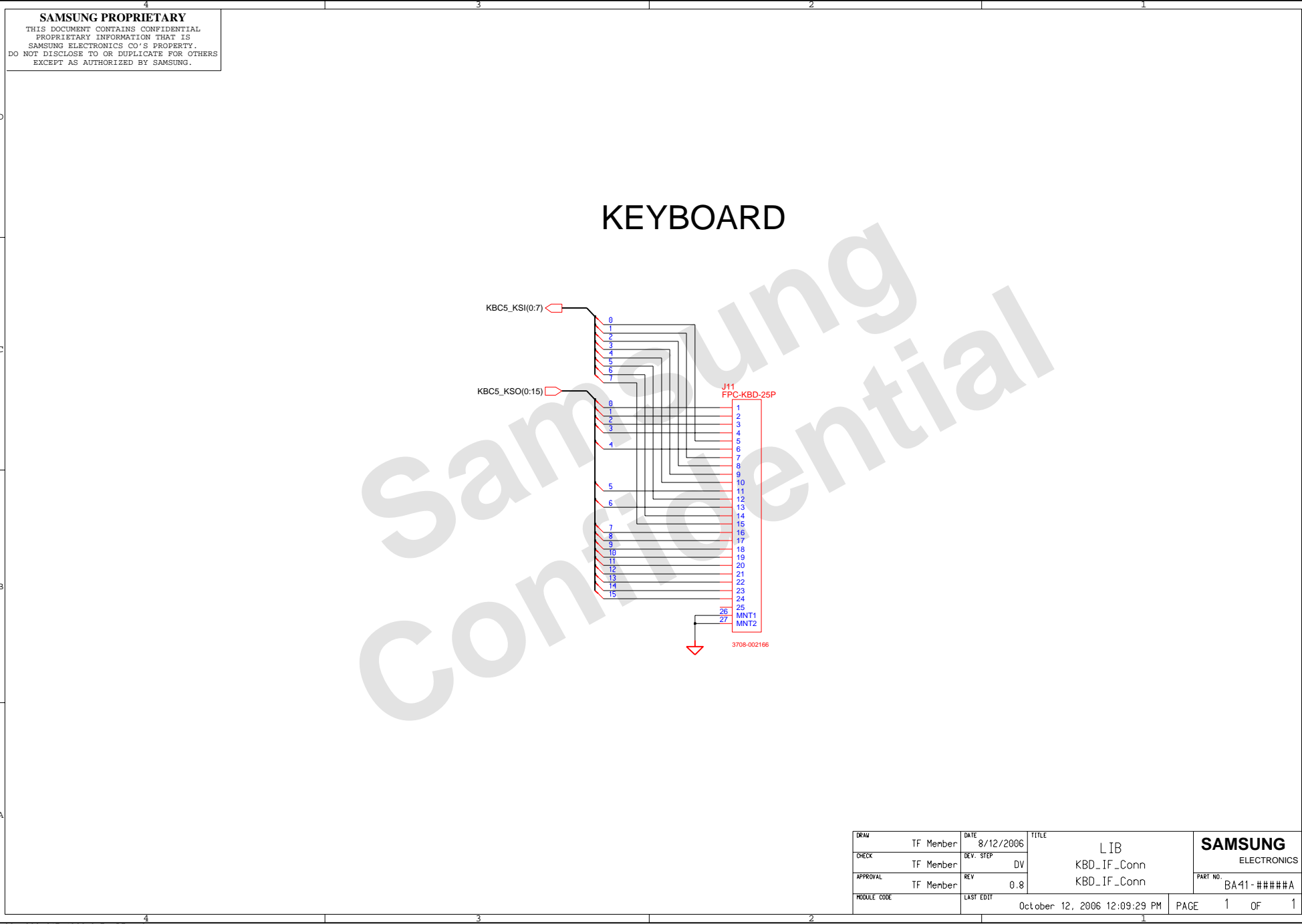


DRAW	TF Member	DATE	TITLE	LIB DMB_IF_Conn DMB_IF_Conn	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	TF Member	DEV. STEP	DV		
APPROVAL	TF Member	REV	0.8		
MODULE CODE	LAST EDIT	October 11, 2006 16:17:06 PM	PAGE 1 OF 1		

TOUCHPAD



DRAW	TF Member	DATE	8/12/2006	TITLE  LIB Touchpad_IF_Conn Touchpad_IF_Conn	<b>SAMSUNG</b> ELECTRONICS
CHECK	TF Member	DEV. STEP	DV		
APPROVAL	TF Member	REV	0.8		
MODULE CODE		LAST EDIT	October 12, 2006 12:11:36 PM		
				PAGE	1 OF 1



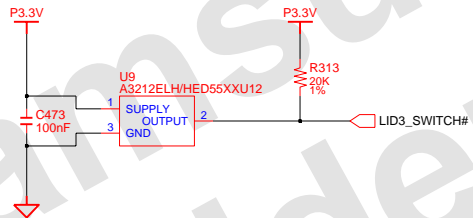
KEYBOARD

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DRAW	TF Member	DATE	8/12/2006	TITLE	L IB	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	KBD_IF_Conn		
APPROVAL	TF Member	REV	0.8	KBD_IF_Conn		
MODULE CODE	LAST EDIT		October 12, 2006 12:09:29 PM		PAGE	1 OF 1

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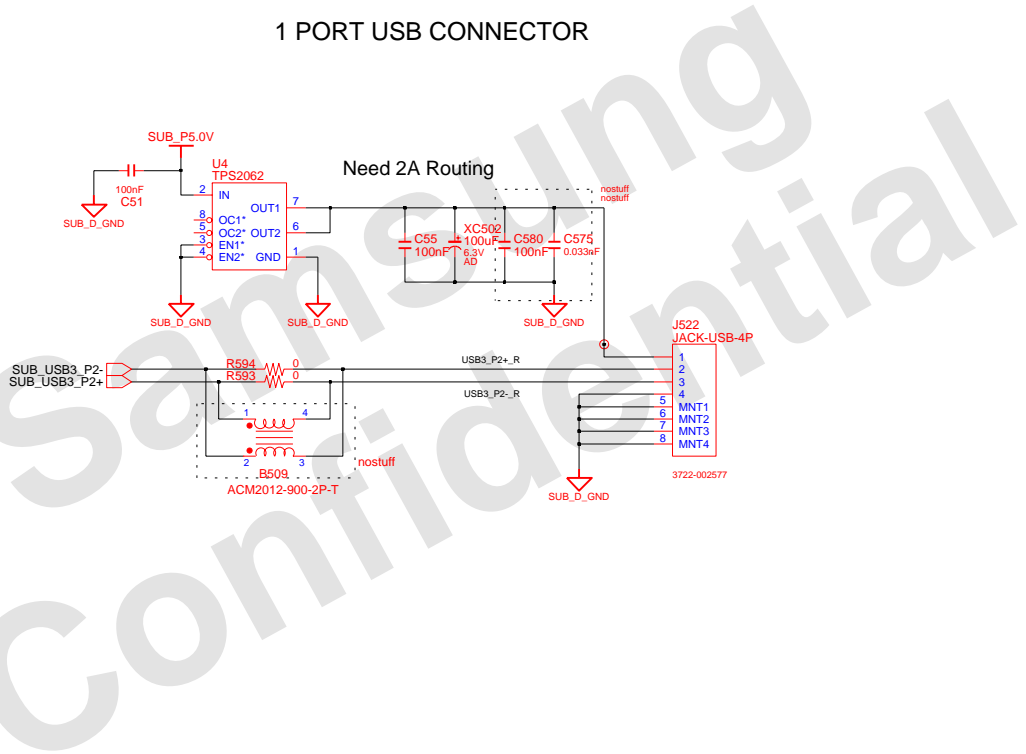
LID\_SWITCH



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	LID_Switch		
APPROVAL	TF Member	REV	0.8	LID_Switch		
MODULE CODE		LAST EDIT	October 12, 2006 12:14:03 PM	PAGE	1 OF 1	PART NO. BA41-####A



1 PORT USB CONNECTOR



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	USB_1Port		
APPROVAL	TF Member	REV	0.8	USB_1Port		
MODULE CODE	LAST EDIT			October 10, 2006 20:57:32 PM	PAGE	1 OF 1

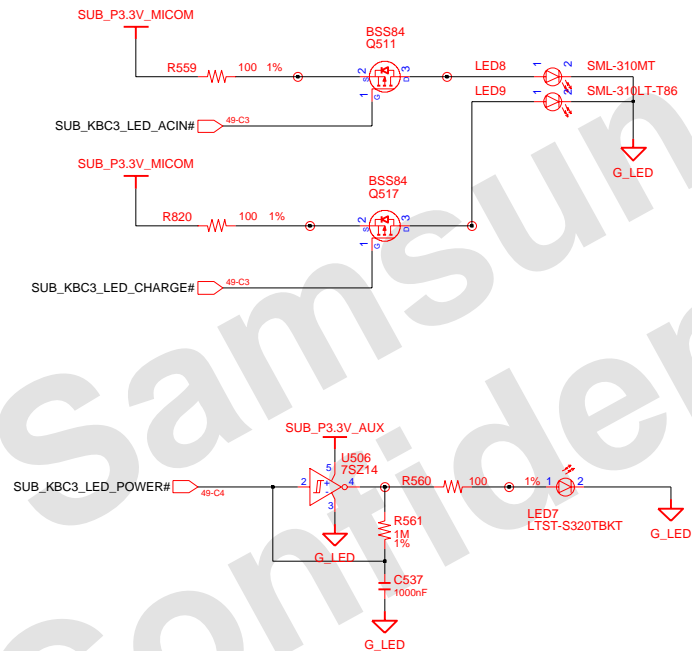




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CHECK	TF Member	DEV. STEP	DV	Other_Debug_80		
APPROVAL	TF Member	REV	0.8	Other_Debug_80		
MODULE CODE		LAST EDIT	October 10, 2006 20:45:09 PM	PAGE	1 OF 1	PART NO. BA41-####A

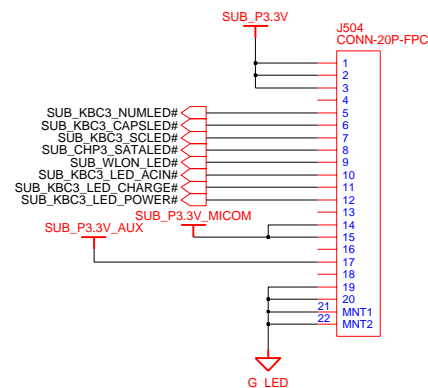
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ADAPTERIN/CHARGING LED



DRAW	TF Menber	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Menber	DEV. STEP	DV	PWR_Charger		
APPROVAL	TF Menber	REV	0.8	PWR_Charger #1		
MODULE CODE		LAST EDIT	October 10, 2006 20:48:53 PM	PAGE	1 OF 2	PART NO. BA41-####A

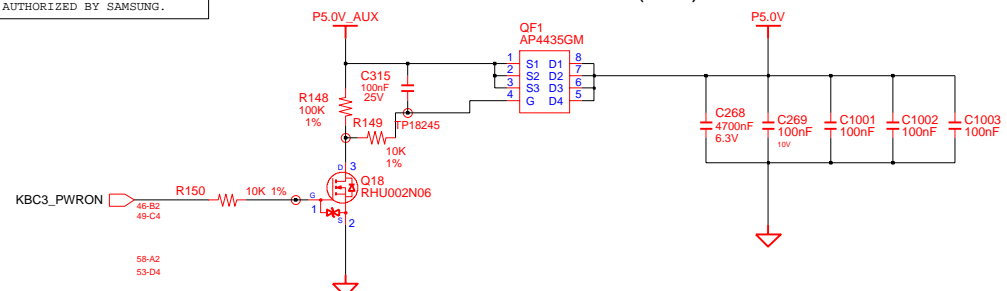
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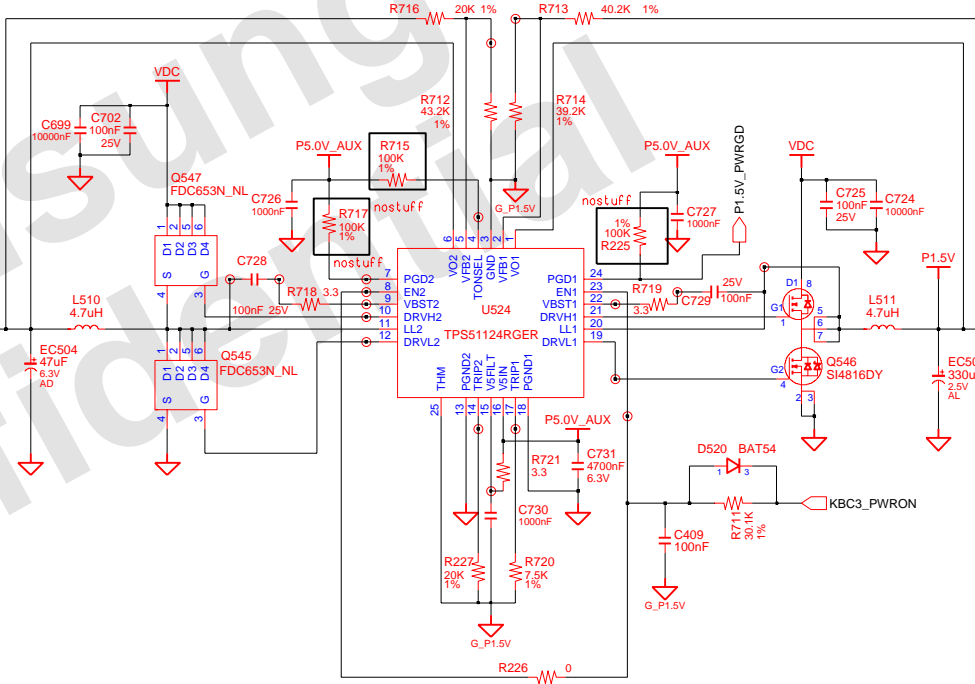
DRAW	TF Member	DATE	8/12/2006	TITLE  LIB LED-Switch LED-Switch	SAMSUNG ELECTRONICS		
CHECK	TF Member	DEV. STEP	DV				
APPROVAL	TF Member	REV	0.8		PART NO.	BA41-#####	
MODULE CODE	LAST EDIT				October 10, 2006 20:43:43 PM	PAGE	1 OF 1

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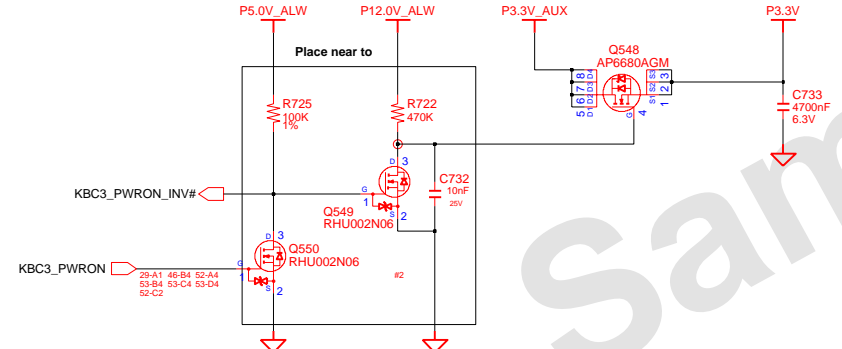
Switched Power On (P5V)



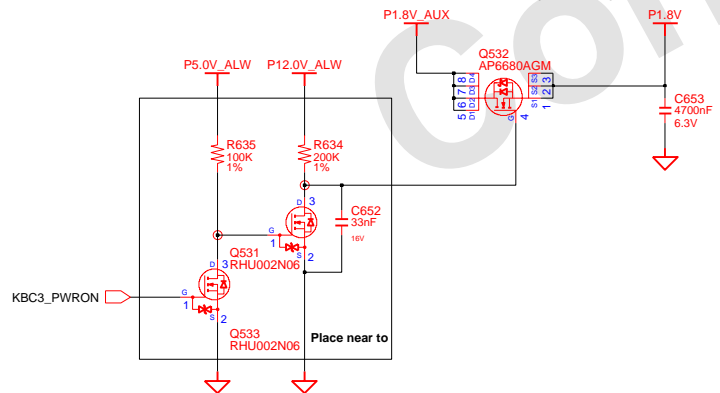
Power (P1.5V & P1.1V)



Switched Power On (P3.3V)



Switched Power On (P1.8V)



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	PWR_Switched		
APPROVAL	TF Member	REV	0.8	PWR_Switched		
MODULE CODE	undef:ned	LAST EDIT	October 10, 2006 20:54:08 PM	PAGE	1 OF 1	

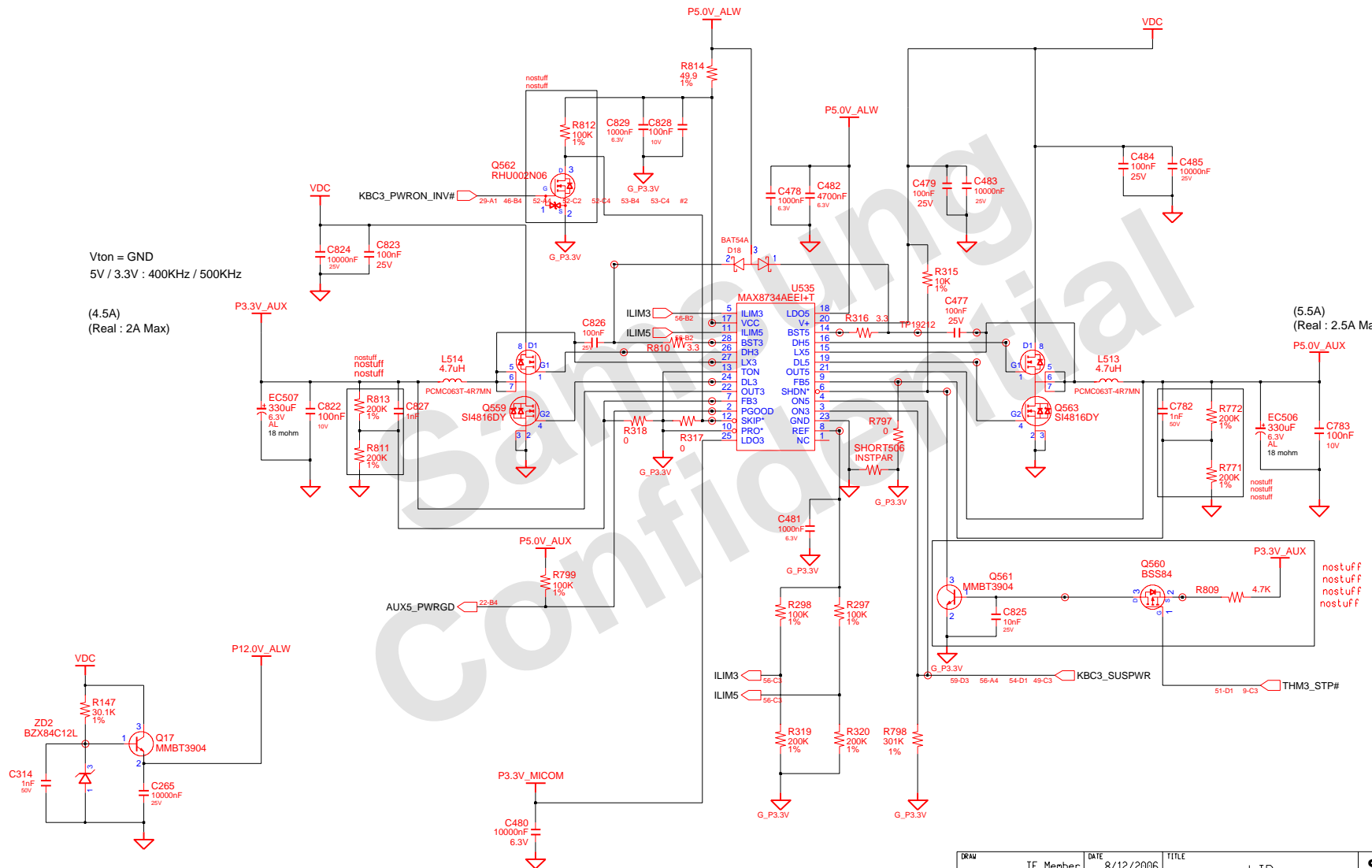


# P3.3V\_ALW/AUX & P5V\_AUX

V<sub>ton</sub> = GND  
5V / 3.3V : 400KHz / 500KHz

(4.5A)  
(Real : 2A Max)

(5.5A)  
(Real : 2.5A Max)

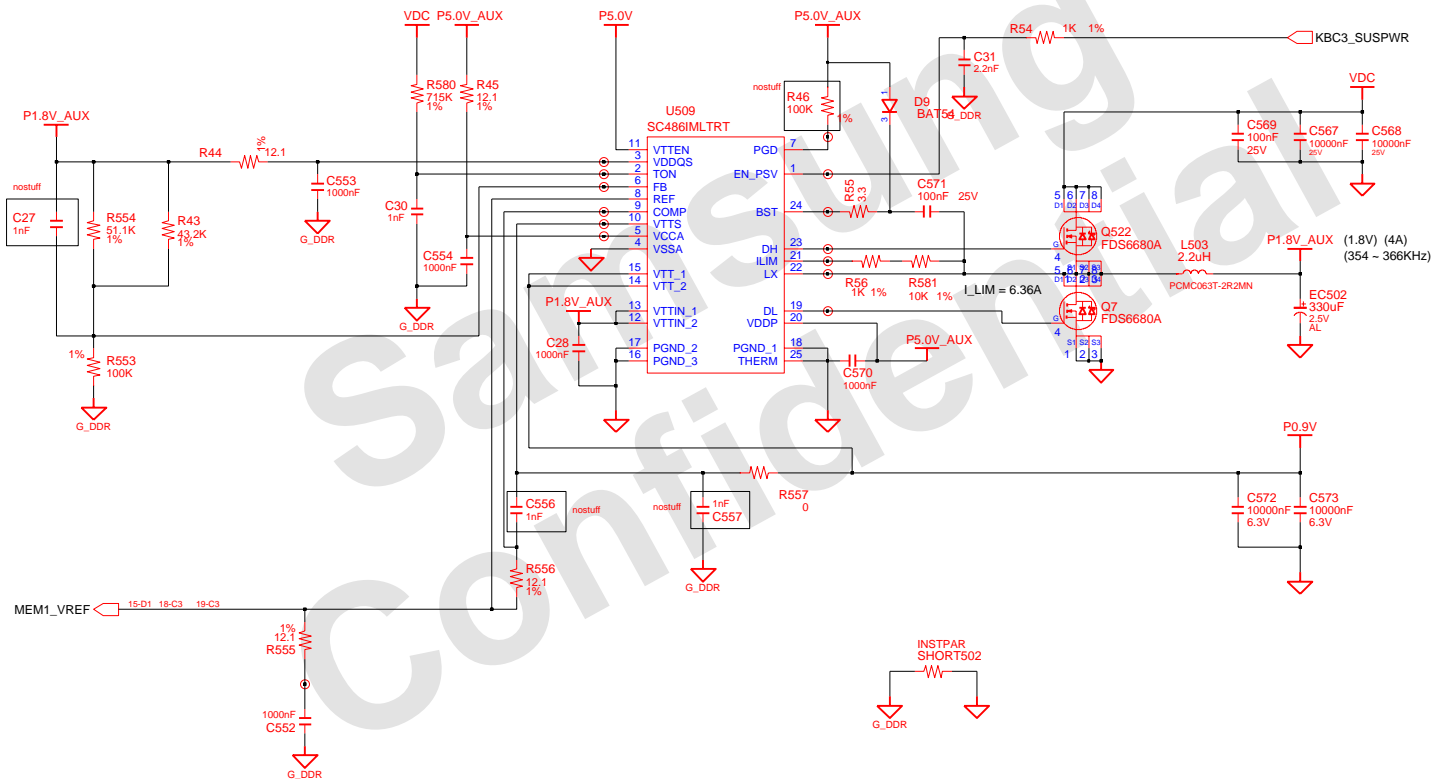


DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV		PWR_3V_5V	
APPROVAL	TF Member	REV	0.8		PWR_3V_5V	
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:47:11 PM	PAGE	1 OF 1	



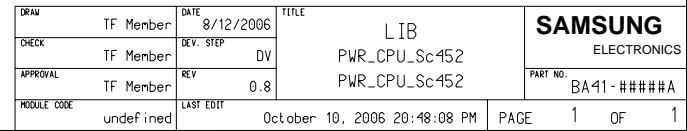


## DDR2 Power



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG
CHECK	TF Member	DEV. STEP	DV	PWR_Memory	PWR_Memory	ELECTRONICS
APPROVAL	TF Member	REV	0.8	PWR_Memory	PWR_Memory	PART NO.
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:52:43 PM	PAGE	1	BA41-####A
				OF	1	

CPU VRM [SEMTECH]



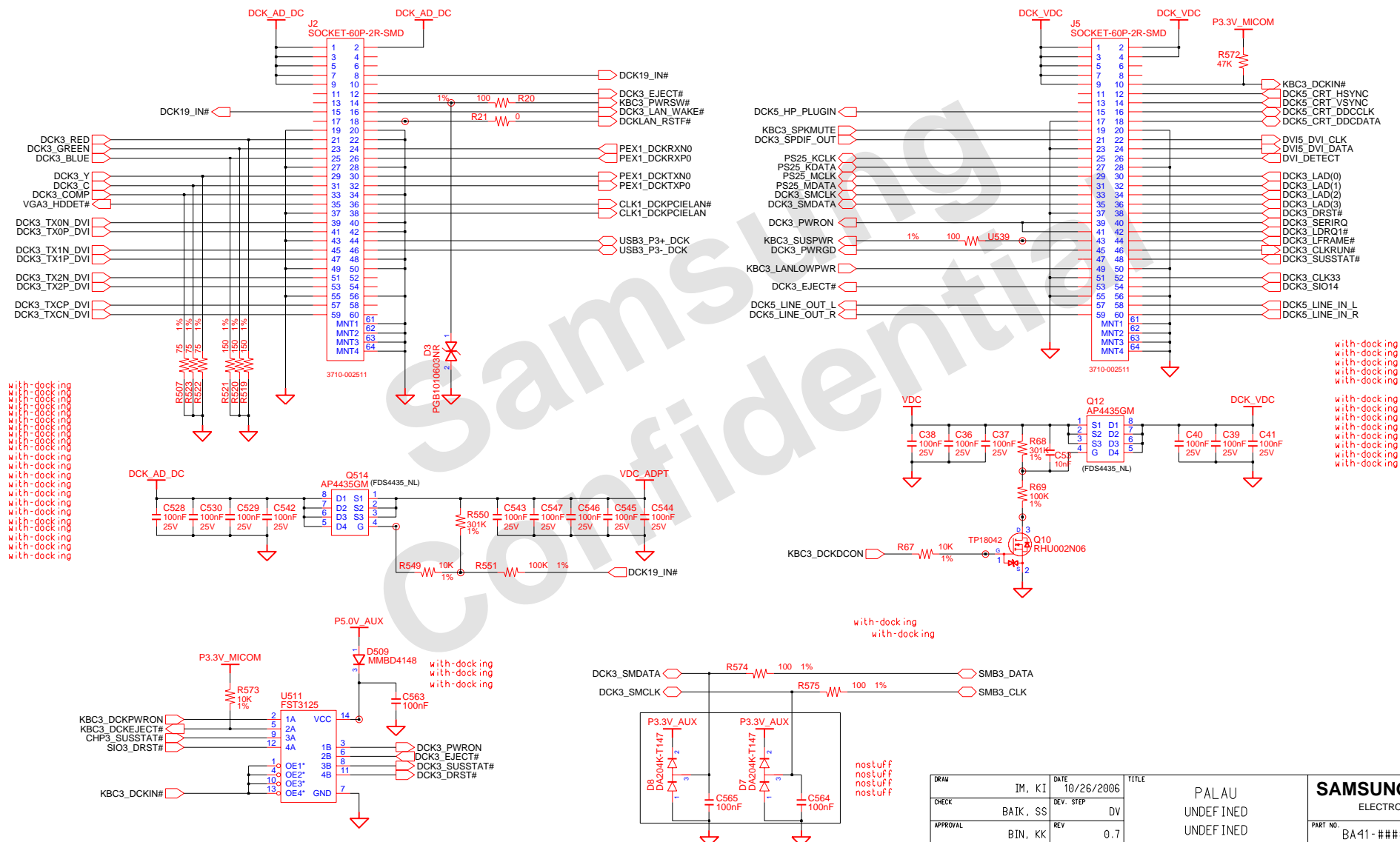


## DOCKING OPTION

### DOCKING CONNECTOR (130PIN)

Docking Placement

PWR1	1	129	PWR4
Top View			
PWR3	2	130	PWR2



DRAW	IM, KI	DATE	10/26/2006	TITLE	PALAU UNDEFINED	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV			PART NO. BA41-#####A
APPROVAL	BIN, KK	REV	0.7			
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	21	OF 22



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TP18673A0UD3_SEL	TP18625CCLK1_PCIEL0M	TP18543ODCK3_LAN_WAKE
TP18674A0UD3_BCLK	TP18626CCLK1_PCIEL0M#	TP18544ODCK3_LDR01#
TP18675A0UD3_BEEP	TP18627CCLK1_PEG	TP18545ODCK3_LFRAME#
TP18676A0UD3_CP100#	TP18628CCLK1_PEG#	TP18546ODCK3_PWRGD
TP18677A0UD3_GPI100#	TP18629CCLK1_PEG#	TP18547ODCK3_TRN
TP18678A0UD3_HP_MUTE	TP18630CCLK1_SATA#	TP18548ODCK3_RED
TP18679A0UD3_RST#	TP18631CCLK3_DGLOPC	TP18549ODCK3_SERIRQ
TP18680A0UD3_S0D10	TP18632CCLK3_GFX_27M	TP18550ODCK3_S1014
TP18681A0UD3_S0D10#	TP18633CCLK3_GFX_27M_SS	TP18551ODCK3_SMLC
TP18682A0UD3_S0D10#	TP18634CCLK3_I2C	TP18552ODCK3_SMT
TP18683A0UD3_SPKR	TP18635CCLK3_PCLK1CH	TP18553ODCK3_SPDITE
TP18684A0UD3_SYNC	TP18636CCLK3_PCLK1NCM	TP18554ODCK3_SUSTOUT#
TP18685A0UD5_HP_0_LEFT	TP18637CCLK3_PCLK3IO3	TP18555ODCK3_TXGN_DVI
TP18686A0UD5_HP_0_RIGHT	TP18638CCLK3_PCLK3IO_DS	TP18556ODCK3_TXGN_DVI
TP18687A0UD5_L1N_1_LEFT	TP18639CCLK3_PCLK3IO_DS	TP18557ODCK3_TXN_DVI
TP18688A0UD5_L1N_0_RIGHT	TP18640CCLK3_S1014	TP18558ODCK3_TXN_DVI
TP18689A0UD5_MICE_LEFT	TP18608CCLK3_USB4#	TP18559ODCK3_TXPD_DVI
TP18690A0UD5_MICE_RIGHT		TP18560ODCK3_TXPD_DVI
TP18691A0UD5_MICE_VREF	TP18597CPU1_A20M#	TP18561ODCK3_TXPD_DVI
TP18692A0UD5_MICE_VREF_RIGHT	TP18598CPU1_A0D5#	TP18562ODCK3_VCRPT_DVI#
TP18693A0UD5_MICE_LEFT	TP18599CPU1_A0D5#	TP18515ODCK3_Y
TP18694A0UD5_MICE_RIGHT	TP18599CPU1_A0D5B0#	TP18516ODCK5_CRT_DCCCL
TP18695A0UD5_MICE_VREF	TP18600CPU1_A0D5B1#	TP18517ODCK5_CRT_DCCCL
TP18696A0UD5_SENS_A	TP18601CPU1_BNR	TP18518ODCK5_CRT_HSVGN
TP18697A0UD5_SENS_HP#	TP18602CPU1_BNR	TP18519ODCK5_CRT_HSVGN
TP18698A0UD5_SENS_LINEIN#	TP18603CPU1_BRED#	TP18520ODCK5_HP_PLUGIN
TP18699A0UD5_SENS_MIC#	TP18604CPU1_BSEL0	TP18521ODCK5_LINE_IN_1
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TP18701BAT3_DETECT#	TP18606CPU1_BSEL2	TP18523ODCK5_LINE_OUT
TP18702BAT3_DETECT#	TP18607CPU1_CPURST#	TP18524ODCK5_LINE_OUT#
TP18703BAT3_VOLT#		TP18525ODCK5_LAN_RST#
TP18704CHP3_BIOSWP#	TP18590CPU1_DBSY#	TP18526ODCK5_VIN1_CLK
TP18641CHP3_BIOSUS_CR#	TP18591CPU1_DEFEK#	TP18527ODV15_DV1_DATA
TP18642CHP3_C0_DATA_0	TP18592CPU1_DEFEK#	TP18528ODCK5_VIN1_DATA
TP18643CHP3_C0_DATA_0	TP18593CPU1_DPSL#	TP18529ODCK5_VPE#
TP18644CHP3_C0_RST#_0	TP18594CPU1_DPW#	TP18530ODCK5_CPUBS#
TP18645CHP3_C0_RST#_1	TP18595CPU1_DRDY#	
TP18646CHP3_C0_PUSP#		
TP18647CHP3_C0_DCKEN	TP18596CPU1_FERR#	TP18508ODCK5_P3BAST#
TP18648CHP3_C0_DCKEN	TP18596CPU1_HIT#	TP18510ODCK5_VIN_DV0
TP18649CHP3_DPPSLPVR	TP18564CPU1_HIT#	TP18511ODCK5_P3BAST
TP18650CHP3_GPI029	TP18565CPU1_I0GNE#	TP18512ODCK5_THRMDIR
TP18651CHP3_GPI030#	TP18566CPU1_I0INT#	TP18513ODCK5_THRMDIR
TP18652CHP3_I0INVDEN#	TP18567CPU1_I0INT#	TP18514ODCK5_THRMDIR#
TP18653CHP3_I0INVMEN	TP18568CPU1_LOCK#	
TP18654CHP3_LAN100_SLP	TP18569CPU1_NMI	TP18505ODCK5(10)
TP18655CHP3_L2DRQ0#	TP18570CPU1_PSI#	TP18506ODCK5(10)
TP18656CHP3_L2DR01#	TP18571CPU1_PWRGDUPU	TP18507ODCK5(11)
TP18657CHP3_P3BAST		TP18508ODCK5(12)
TP18658CHP3_TRICRST#	TP18572CPU1_RS0#	TP18503ODCK5(13)
TP18659CHP3_SATACLKREQ#	TP18573CPU1_RS1#	TP18504ODCK5(10,9)
TP18660CHP3_SATALED#		
TP18661CHP3_SERIRQ	TP18574CPU1_RS2#	
TP18662CHP3_S0D10#	TP18575CPU1_RS#	
TP18663CHP3_SLP5#	TP18576CPU1_S1#	TP18444ODIE5_A0
TP18664CHP3_SUSTSTAT#	TP18577CPU1_STPCLK#	TP18445ODIE5_A1
TP18665CCLK0_HCLG0	TP18578CPU1_TCK	TP18446ODIE5_A2
TP18666CCLK0_HCLG0#	TP18579CPU1_T0	TP18447ODIE5_CS#
TP18667CCLK0_HCLG1	TP18580CPU1_THERMP1P	TP18412ODIE5_CS#3
TP18668CCLK0_HCLG1#	TP18581CPU1_TMS	TP18413ODIE5_CS#4
TP18669CCLK1_DCKPCIELAN	TP18582CPU1_TRDY#	TP18414ODIE5_D1
TP18670CCLK1_DCKPCIELAN#	TP18583CPU1_TRST#	TP18415ODIE5_D1(10)
TP18671CCLK1_MCH3GPLL	TP18584CPU1_VCCSENSE	TP18416ODIE5_D1(11)
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TP18609CCLK1_MCH3GPLL	TP18586CPU2_THERMDA	TP18418ODIE5_D1(13)
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TP18611CCLK1_MCLK1	TP18588CPU3_THERMP1P	TP18420ODIE5_D1(15)
TP18612CCLK1_MCLK3P	TP18589CCLK3_IN_IN#	TP18421ODIE5_D2
TP18613CCLK1_MCLK3P#	TP18591CCLK3_K0	TP18422ODIE5_D3
TP18614CCLK1_MCLK3#	TP18592CCLK3_K1	TP18423ODIE5_D4
TP18615CCLK1_MCLK4	TP18593CCLK3_K2	TP18424ODIE5_D5
TP18616CCLK1_MCLK4#	TP18594CCLK3_K3	TP18425ODIE5_D6
TP18617CCLK1_MIN1P1CIE	TP18595CCLK3_K4	TP18426ODIE5_D7

TP18543 DCKC3_LAN_WAKE#	TP18835 OILIM3
TP18544 DCKC3_LDR01#	TP18836 OILIM5
TP18545 DCKC3_LFRAME#	TP18837 KBKC3_A20G
TP18546 DCKC3_WGRD	TP18838 KBKC3_BKL_TON
TP18547 DCKC3_PERSO	TP18839 KBKC3_PERSW#
TP18548 DCKC3_LED	TP18840 KBKC3_CAPLED#
TP18549 DCKC3_SERIO	TP18841 KBKC3_CHGEN
TP18550 DCKC3_SJ014	TP18842 KBKC3_CHKPRSW#
TP18551 DCKC3_CK_K	TP18843 KBKC3_CUPUST#
TP18552 DCKC3_CK_K	TP18844 KBKC3_CDC_CCT#
TP18553 DCKC3_SPDIF_OUT	TP18781 KBKC3_DCK_IN#
TP18554 DCKC3_SSUSAT#	TP18782 KBKC3_EXTISM#
TP18555 DCKC3_TXDN_DVI	TP18783 KBKC3_LANLOWPW
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TP18558 DCKC3_TXYP_DVI	TP18786 KBKC3_LED_CHARGE#
TP18559 DCKC3_TXN2_DVI	TP18787 KBKC3_LED_POWER#
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TP18515 DCKC3_Y	TP18791 KBKC3_PWRON
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TP18520 DCKC5_HWP_PLUGIN	TP18796 KBKC3_RST#
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TP18522 DCKC5_LLINE_IN_R	TP18798 KBKC3_SCLEDD
TP18523 DCKC5_LLINE_IN_R	TP18799 KBKC3_SCMATA#
TP18524 DCKC5_LLINE_OUT_R	TP18800 KBKC3_SCMATA#
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TP18526 DCV15_DVI_CLK	TP18802 KBKC3_THERM_SMCLK
TP18527 DCV15_DVI_DATA	TP18803 KBKC3_THERM_SMDATA
TP18528 DCV15_DVI_DATA	TP18804 KBKC3_THERM_SMDATA
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TP18530 CEXP3_CUPUS#	TP18806 KBKC5_KS1(0)
	TP18807 KBKC5_KS1(1)
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TP18513 CGF3_X2_THRM0P	TP18757 KBKC5_KS1(7)
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TP18504 CPG10(9)	TP18765 KBKC5_KS1(15)
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TP18844 IDIES_A0	TP18767 KBKC5_KS1(17)
TP18845 IDIES_A1	TP18768 KBKC5_KS1(18)
TP18846 IDIES_A2	TP18769 KBKC5_KS1(19)
TP18847 IDIES_C51#	TP18770 KBKC5_KS1(20)
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TP18816 IDIES_D10	TP18773 KBKC5_KS1(23)
TP18817 IDIES_D11	TP18774 KBKC5_KS1(24)
TP18818 IDIES_D12	TP18775 KBKC5_KS1(25)
TP18819 IDIES_D13	TP18776 CLANC3_ACTLED#
TP18820 IDIES_D14	TP18777 CLANC3_LINK100#
TP18821 IDIES_D15	TP18778 CLANC3_LINK100_100#
TP18822 IDIES_D16	TP18779 CLANC3_VPDCLK
TP18823 IDIES_D17	TP18780 CLANC3_VPDCLK
TP18824 IDIES_D18	TP18781 CLANC3_VPDCLK
TP18825 IDIES_D19	TP18782 CLANC3_VPDCLK
TP18826 IDIES_D20	TP18783 CLANC3_VPDCLK
TP18827 IDIES_D21	TP18784 CLANC3_VPDCLK
TP18828 IDIES_D22	TP18785 CLANC3_VPDCLK
TP18829 IDIES_D23	TP18786 CLANC3_VPDCLK
TP18830 IDIES_D24	TP18787 CLANC3_VPDCLK
TP18831 IDIES_IDES_IRQ	TP18788 CLANC3_VPDCLK
TP18832 IDIES_IDES_IRQ	TP18789 CLANC3_VPDCLK
TP18833 IDIES_IDES_IRQ	TP18790 CLANC3_VPDCLK
TP18834 IDIES_IDES_IRQ	TP18791 CLANC3_VPDCLK

P1781835 OILIM3  
 P1781836 OILIM5  
 P1781837 OCBK5.A20C  
 P1781838 OCBK5.BCL.TON  
 P1781839 OCBK5.CAP.PRSW#  
 P1781840 OCBK5.CAPLED#  
 P1781841 OCBK5.CHGEN  
 P1781842 OCBK5.CHK.PRSW#  
 P1781843 OCBK5.CURKST#  
 P1781844 OCBK5.DC.LOCTH  
 P1781845 OCBK5.DCK.LIN  
 P1781846 OCBK5.EXTSMJ#  
 P1781847 OCBK5.LANLOWPHR  
 P1781848 OCBK5.LAN.WAKE  
 P1781849 OCBK5.LED.CHARGE#  
 P1781850 OCBK5.LED.POWER#  
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 P1781852 OCBK5.NETBEN#  
 P1781853 OCBK5.PWRON.PRSW#  
 P1781854 OCBK5.PWRON  
 P1781855 OCBK5.PWRON\_INV#  
 P1781856 OCBK5.PRSW5#  
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 TP18737CMDC3\_MSDATA2\_SDP  
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 TP18740CMDC3\_SDCCLK#  
 TP18741CMDC3\_SODCL\_MSPBS  
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 TP18744CMDC3\_SDDATA2  
 TP18745CMDC3\_SDDATA3  
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 TP18748CMDC3\_XDCD#  
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 TP18763CMCH3\_BMUSY#  
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 TP18765CMCH3\_CKREF#  
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 TP18767CMCH3\_EXTI1S#  
 TP18768CMCH3\_CHSYSYNC#  
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 TP18770CMDC3\_CRT\_SYNC  
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 TP18772CMDC3\_SDI0  
 TP18773CMDC3\_CRT\_GREEN  
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 TP18868PEGC3\_CRT\_HSYNC  
 TP18869PEGC3\_CRT\_RED  
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 TP18874PEGC3\_LED\_VD0DON  
 TP18875PEGC3\_THMS\_CLK  
 TP18876PEGC3\_THMS\_DATA  
 TP18921CPIC3\_18V\_AUX  
 TP18922CPIC3\_18V\_AUX  
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 TP188780 PE65, CRT\_DOC  
 TP188789 PE65, CRT\_HSY  
 TP188805 PE65, CRT\_HSY  
 TP188815 PE65, HDMI\_1L  
 TP188822 PE65, HDMI\_1L  
 TP188833 PE65, TMSD\_1L  
 TP188844 PE65, TMSD\_1L  
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 TP18886 PE65, DCKRNP0  
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 TP188891 PE65, RST\_PST1  
 TP18890 PE65, RST\_RSTOR  
 TP18891 PE65, KCLK  
 TP18892 PE65, KDATA  
 TP18893 PE65, MCLK  
 TP18894 PE65, MDATA  
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 TP18897 CS1M\_C3  
 TP18898 CS1M\_C4  
 TP18899 CS1M\_C6  
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 TP18903 CSMB3\_ALERT#  
 TP18904 CSMB3\_CLK  
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 TP18906 CSMB3\_ME\_CLK  
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